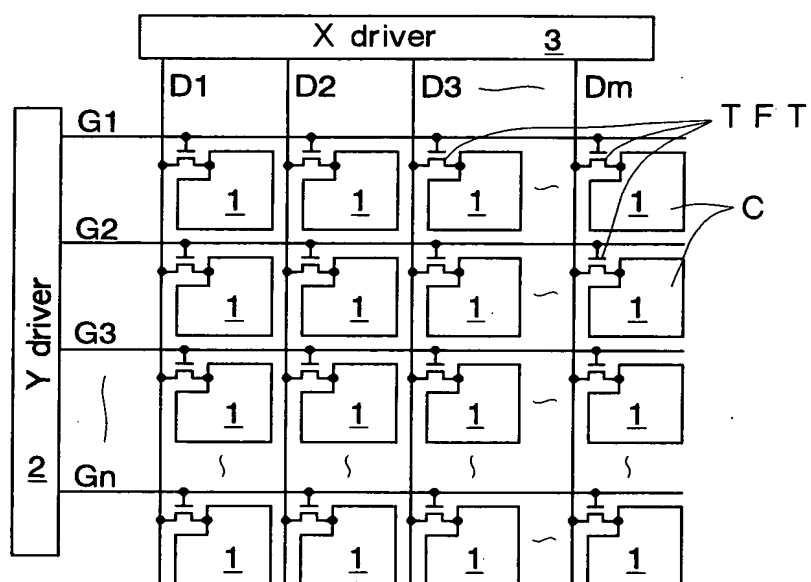
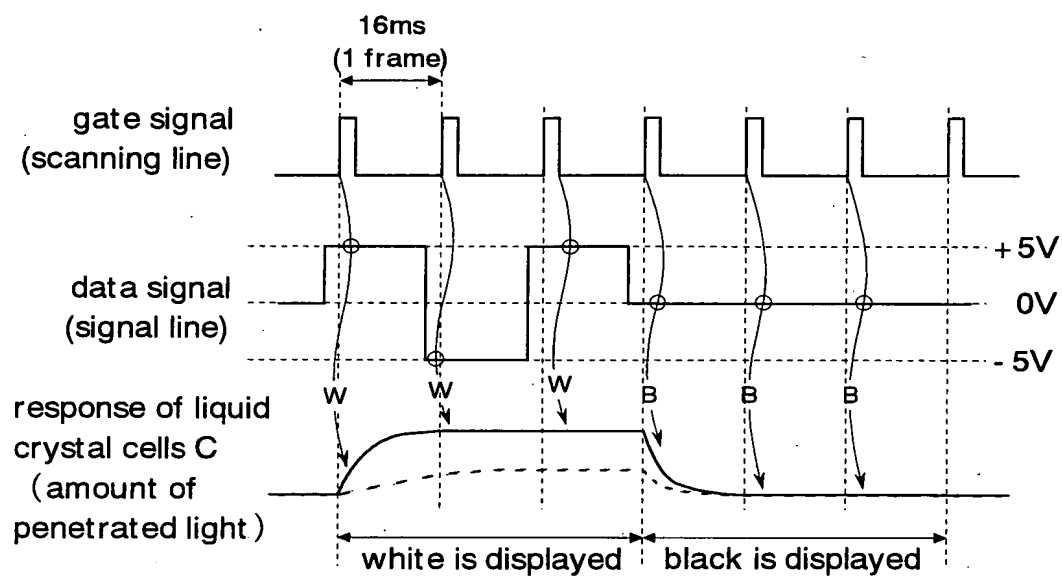


## Prior Art



**Fig. 1**

## Prior Art

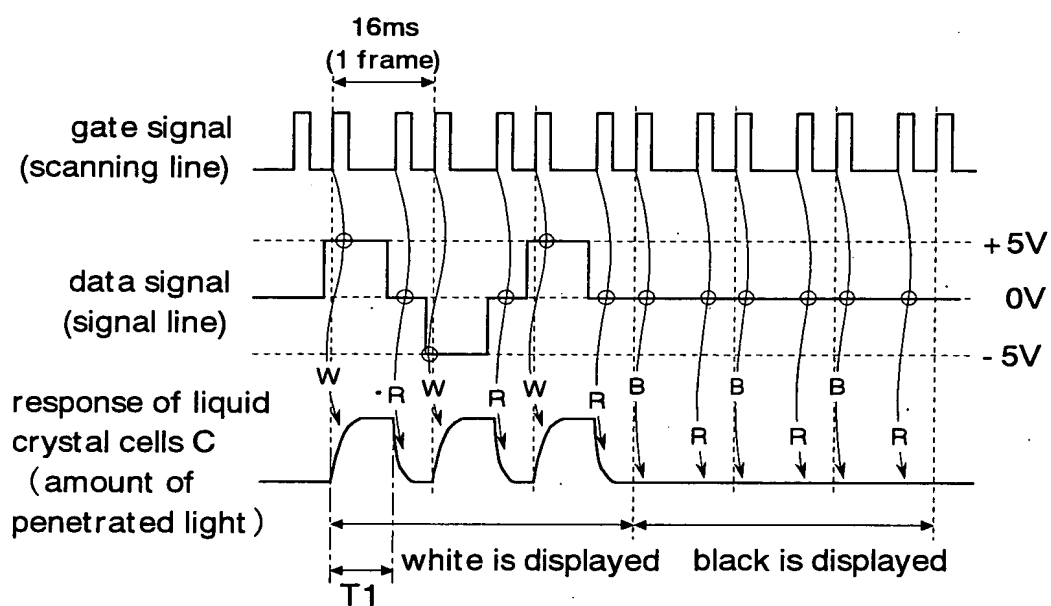


**Fig. 2**

## Prior Art

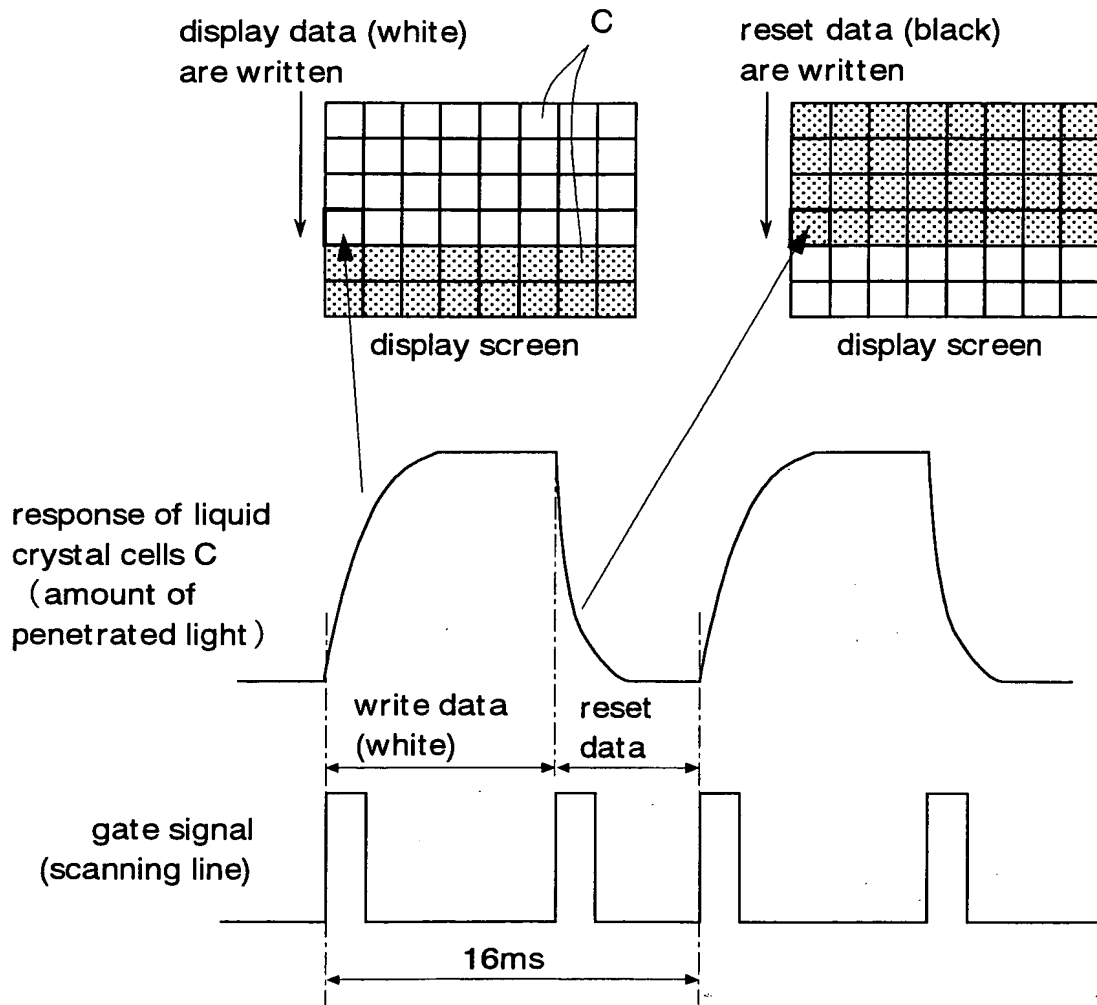


## Prior Art

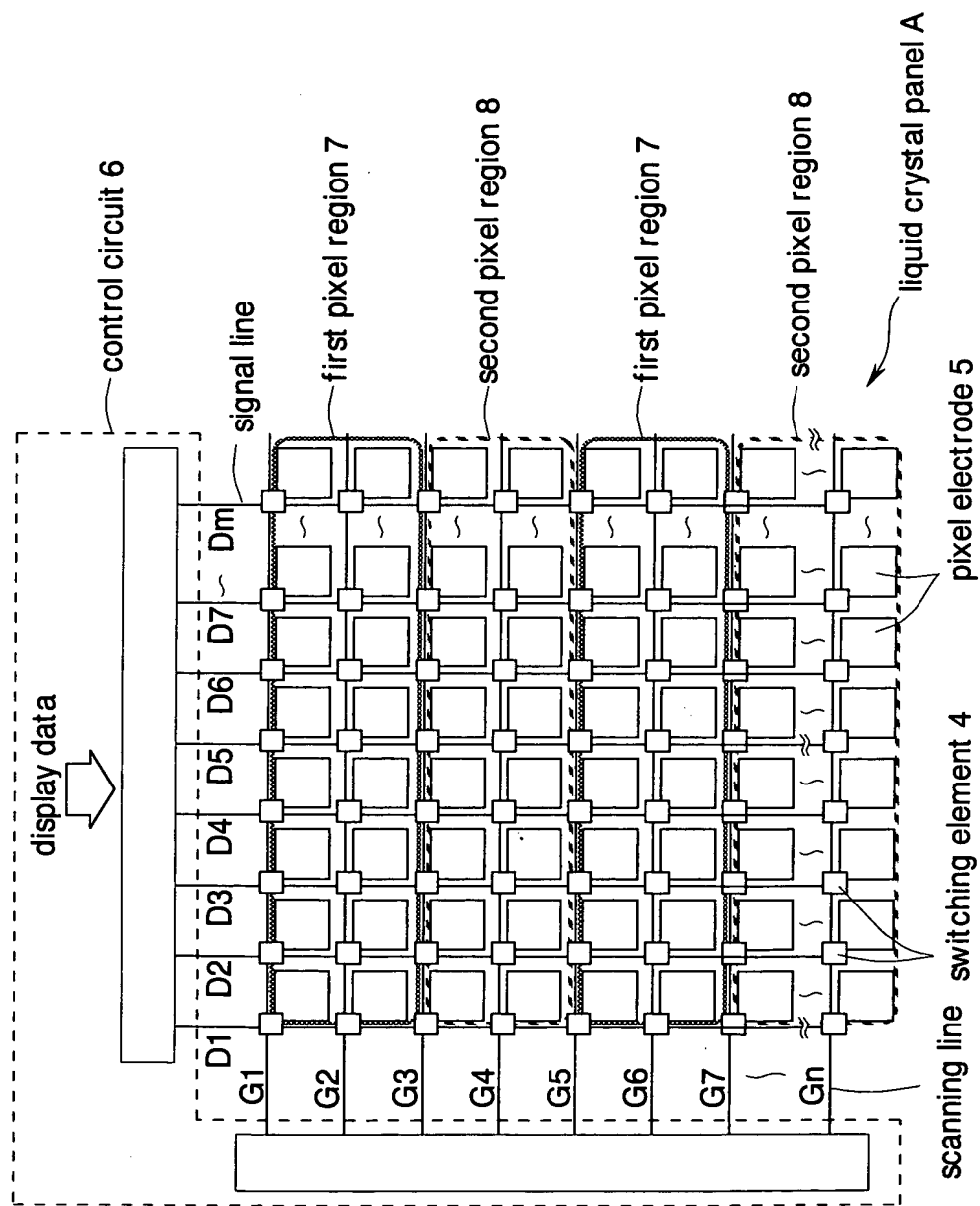


**Fig. 4**

## Prior Art



**Fig. 5**



**Fig. 6**

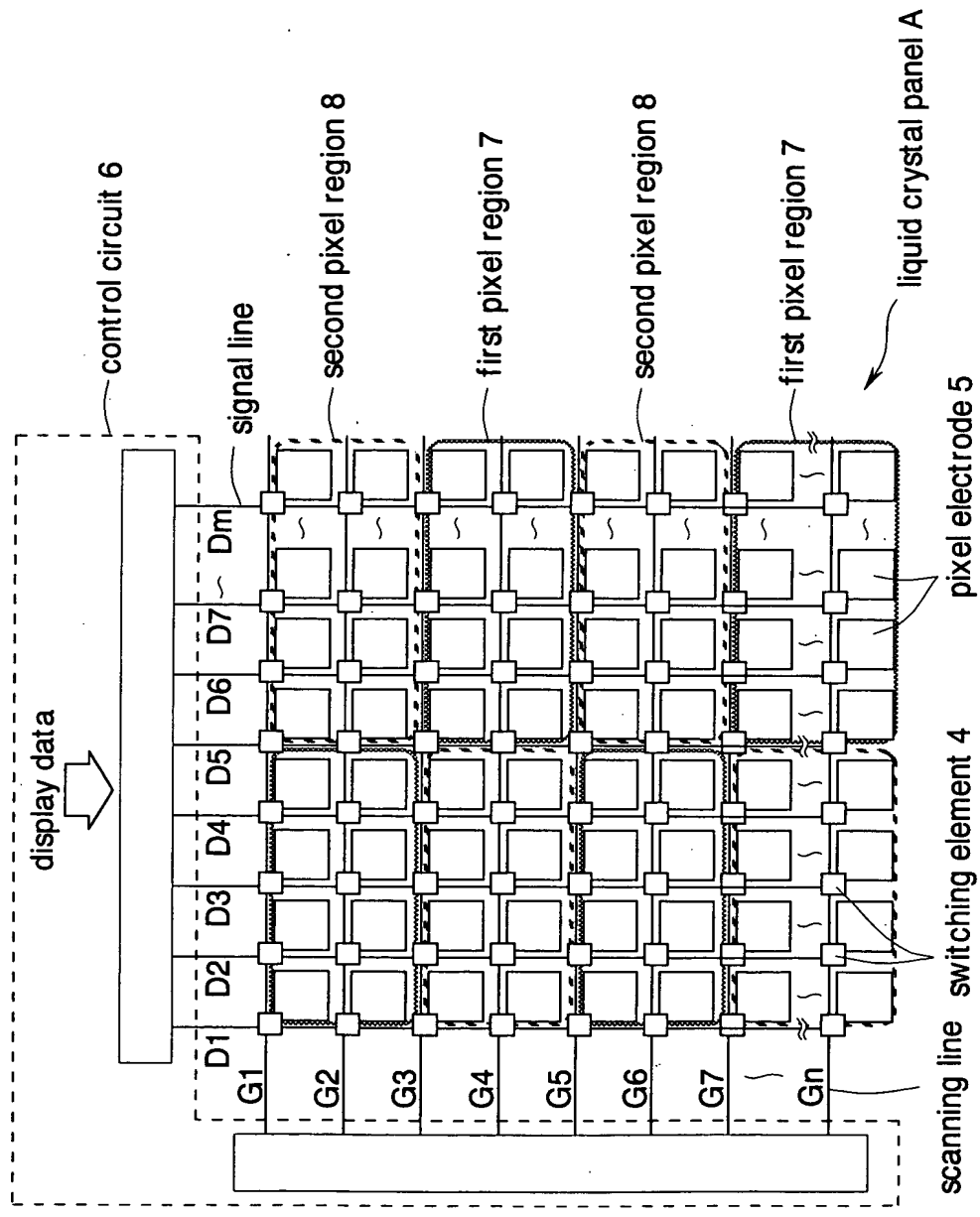


Fig. 7

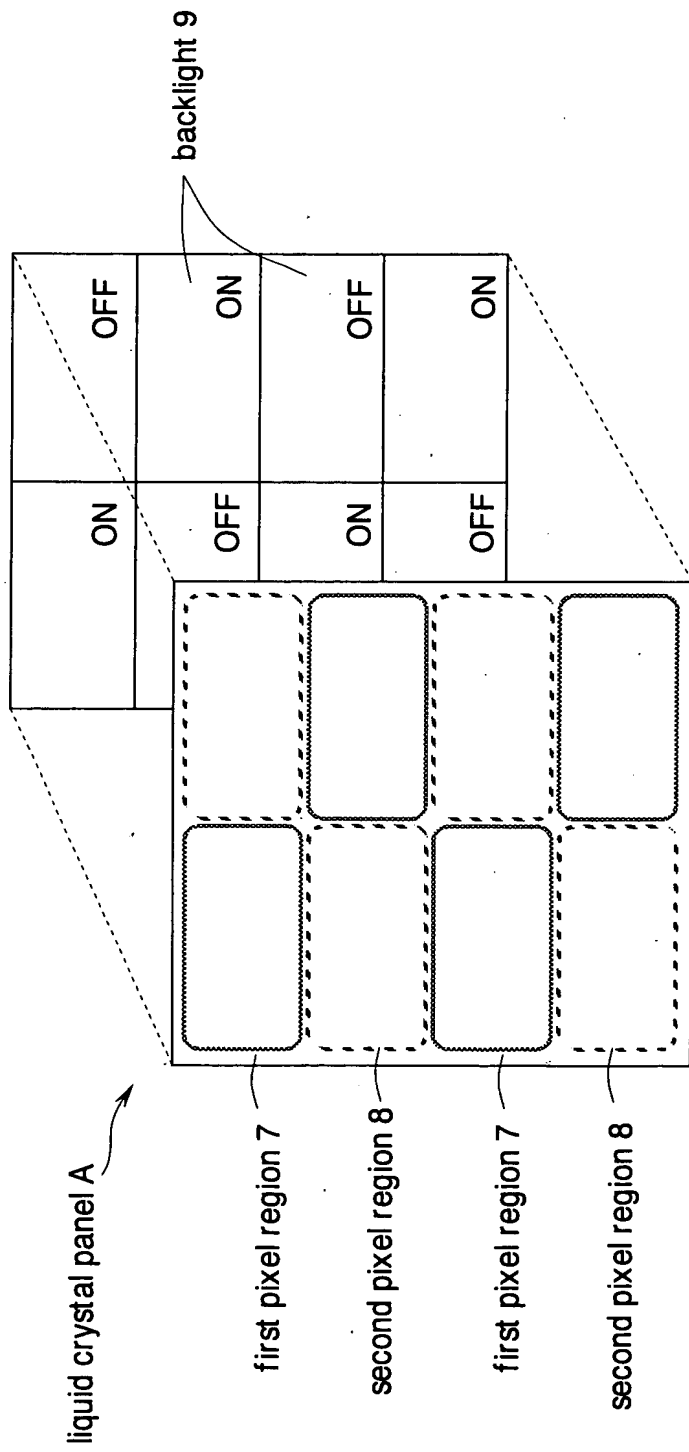


Fig. 8



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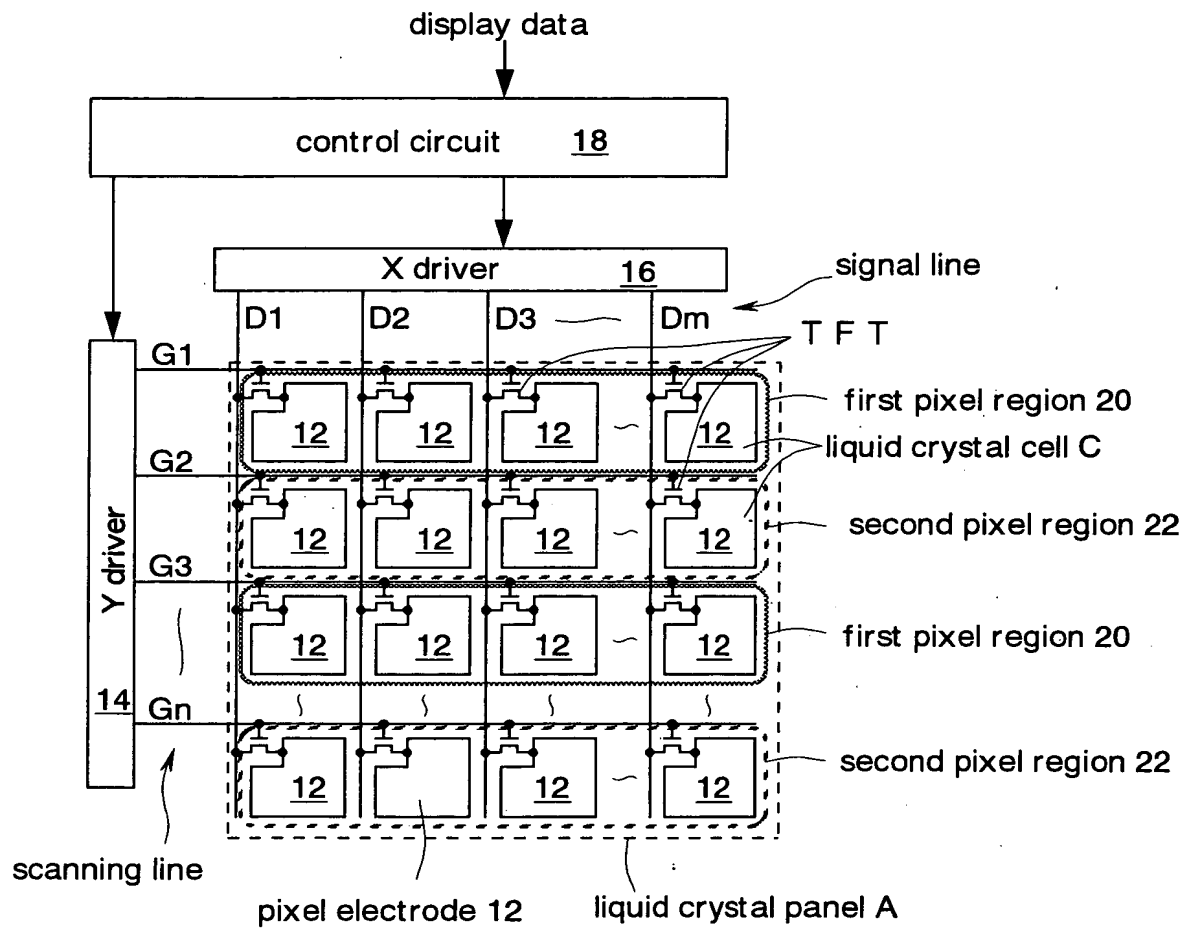


Fig. 9



Fig. 11

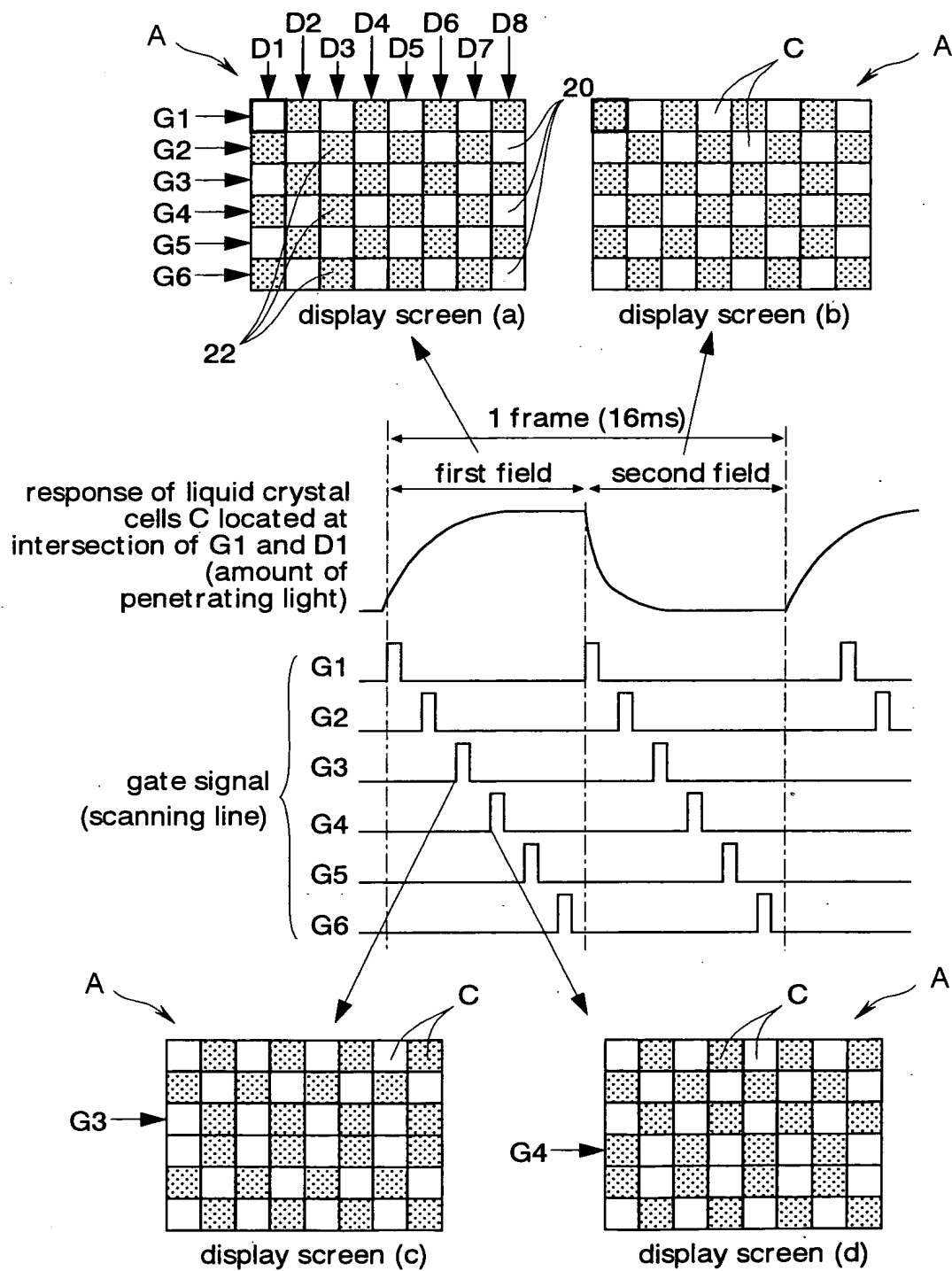
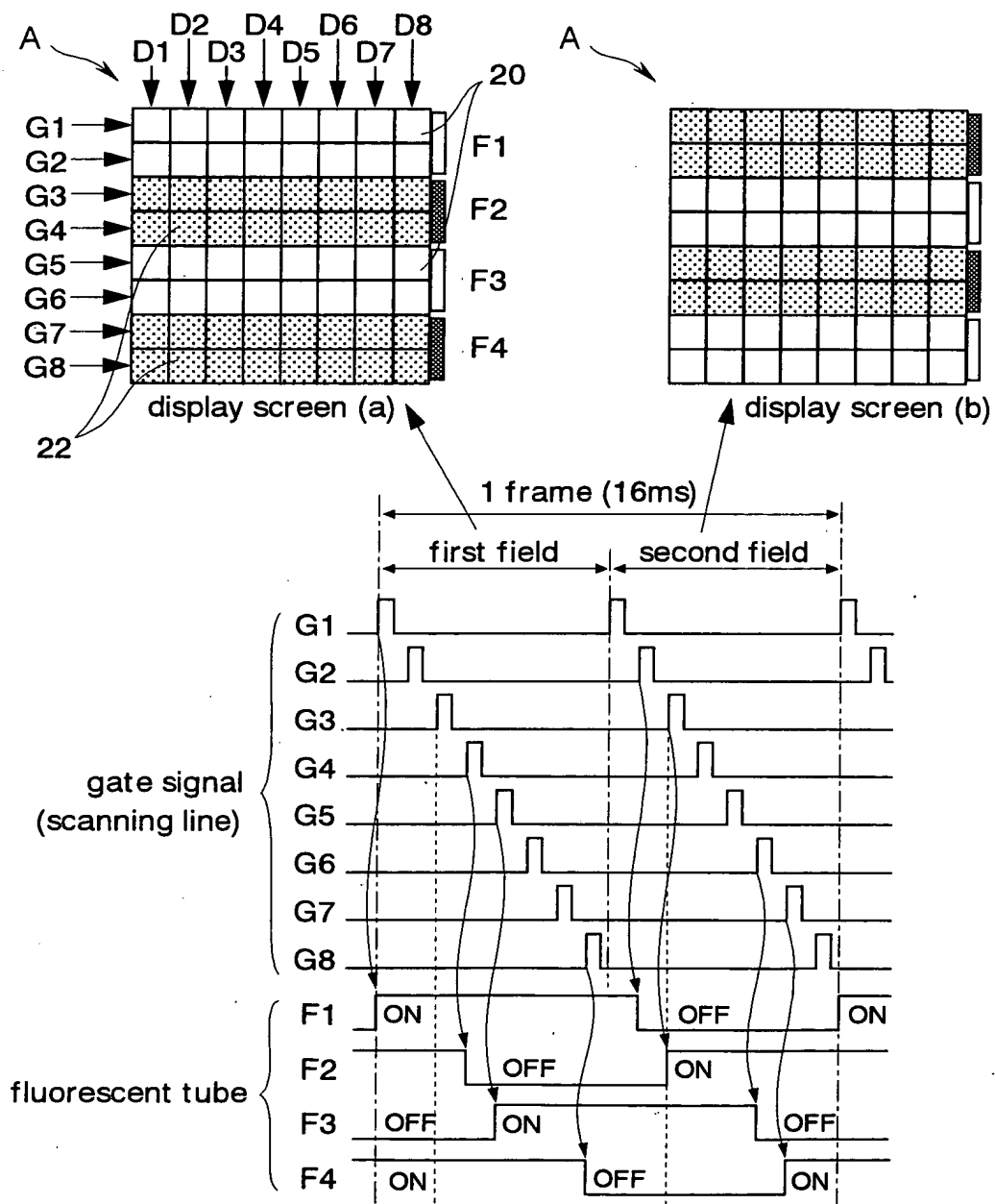


Fig. 12





**Fig. 14**

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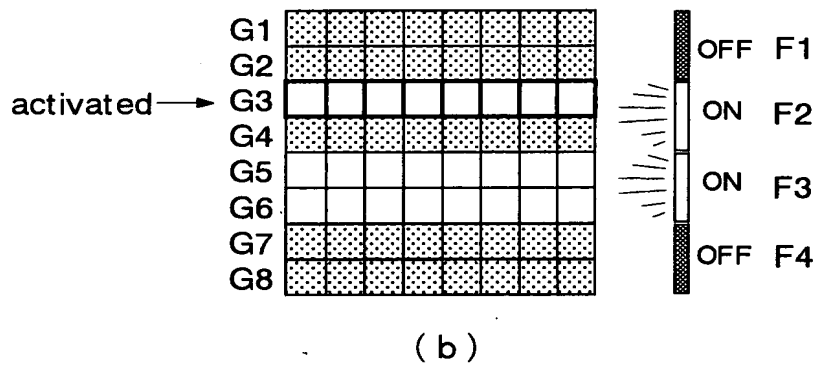
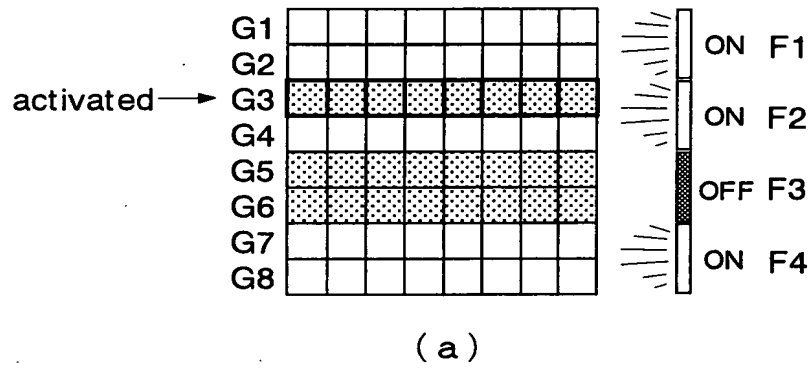
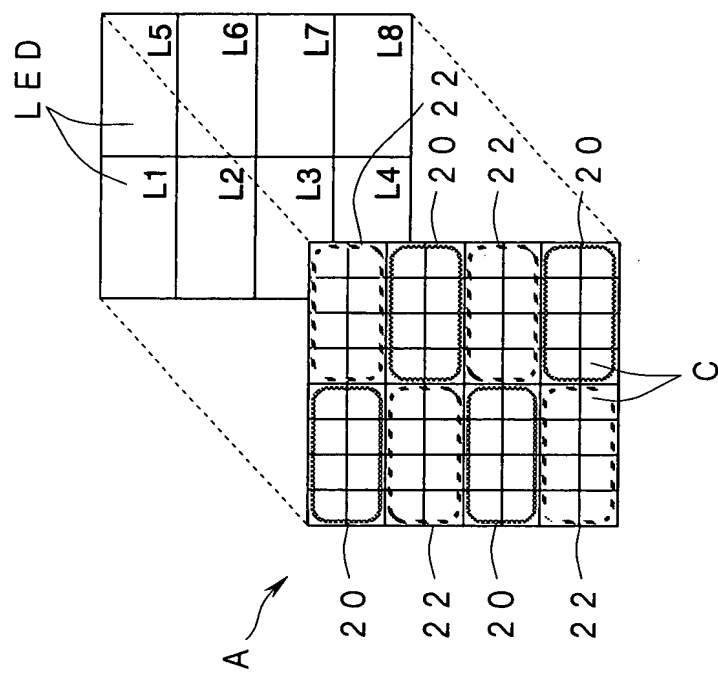


Fig. 15



**Fig. 16**



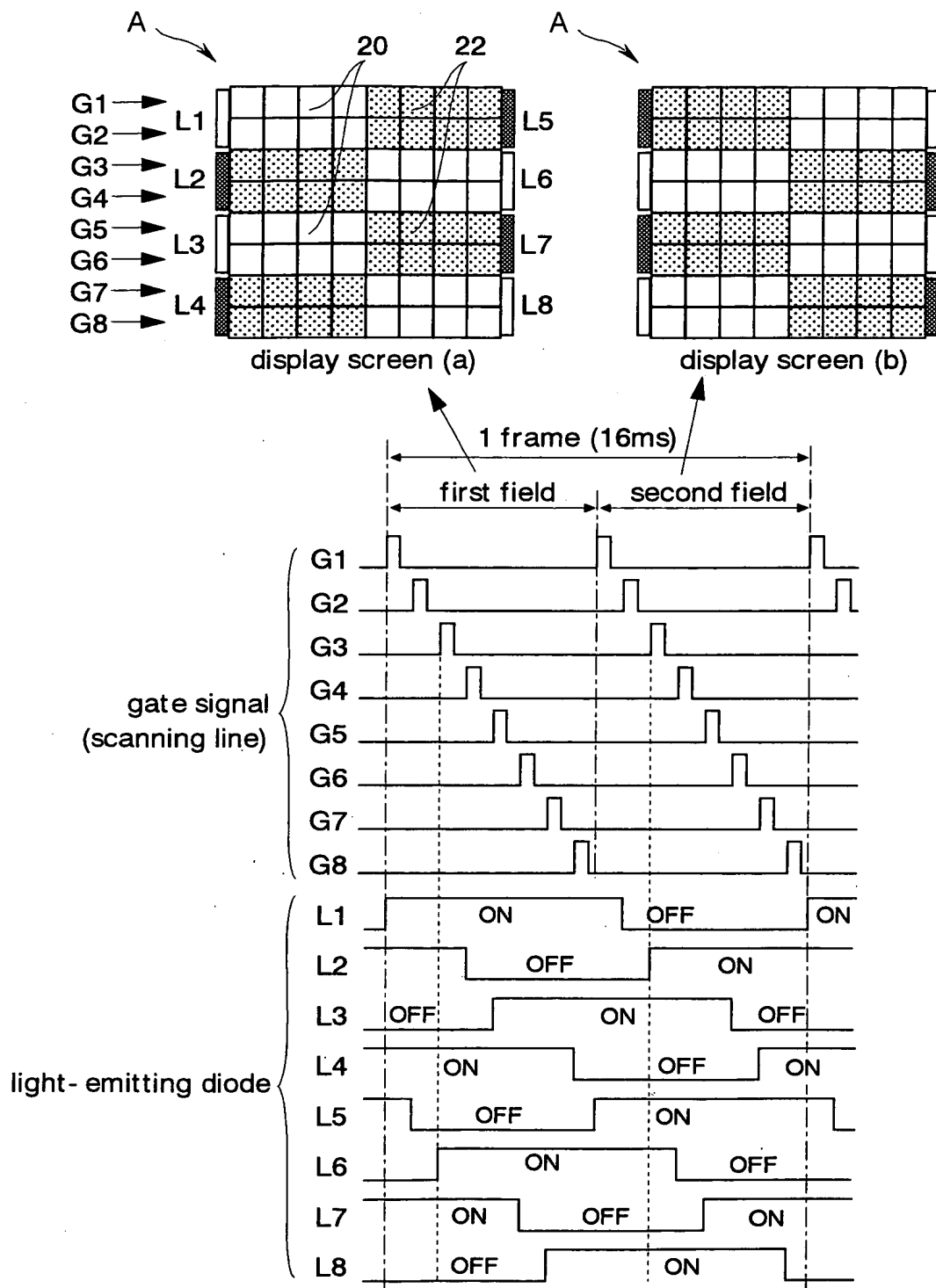


Fig. 17

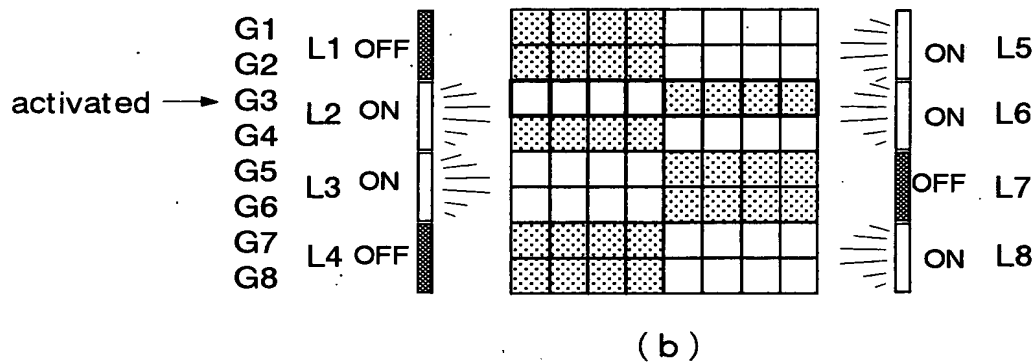
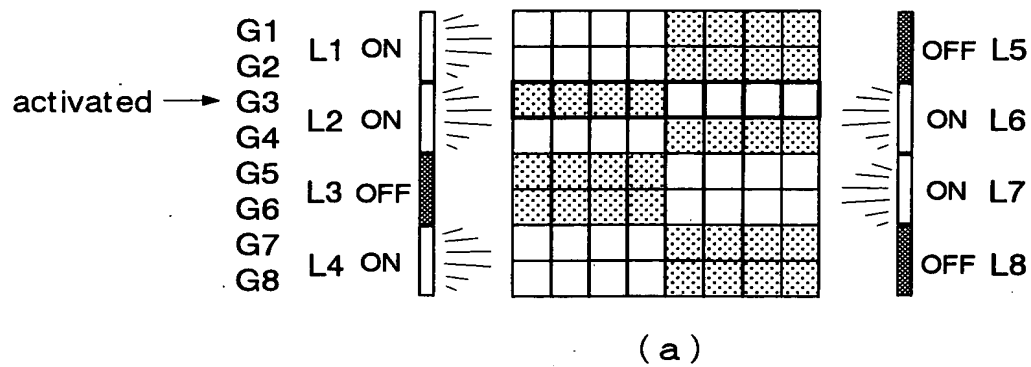


Fig. 18

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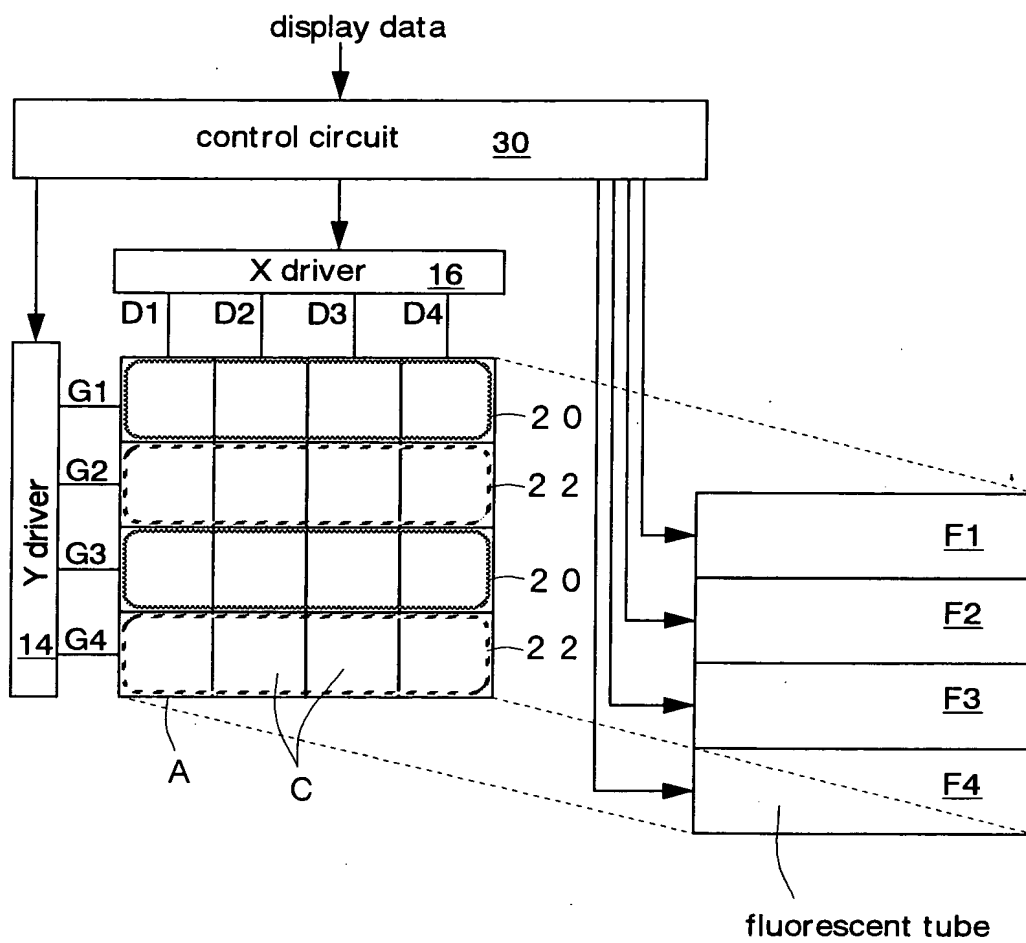


Fig. 19

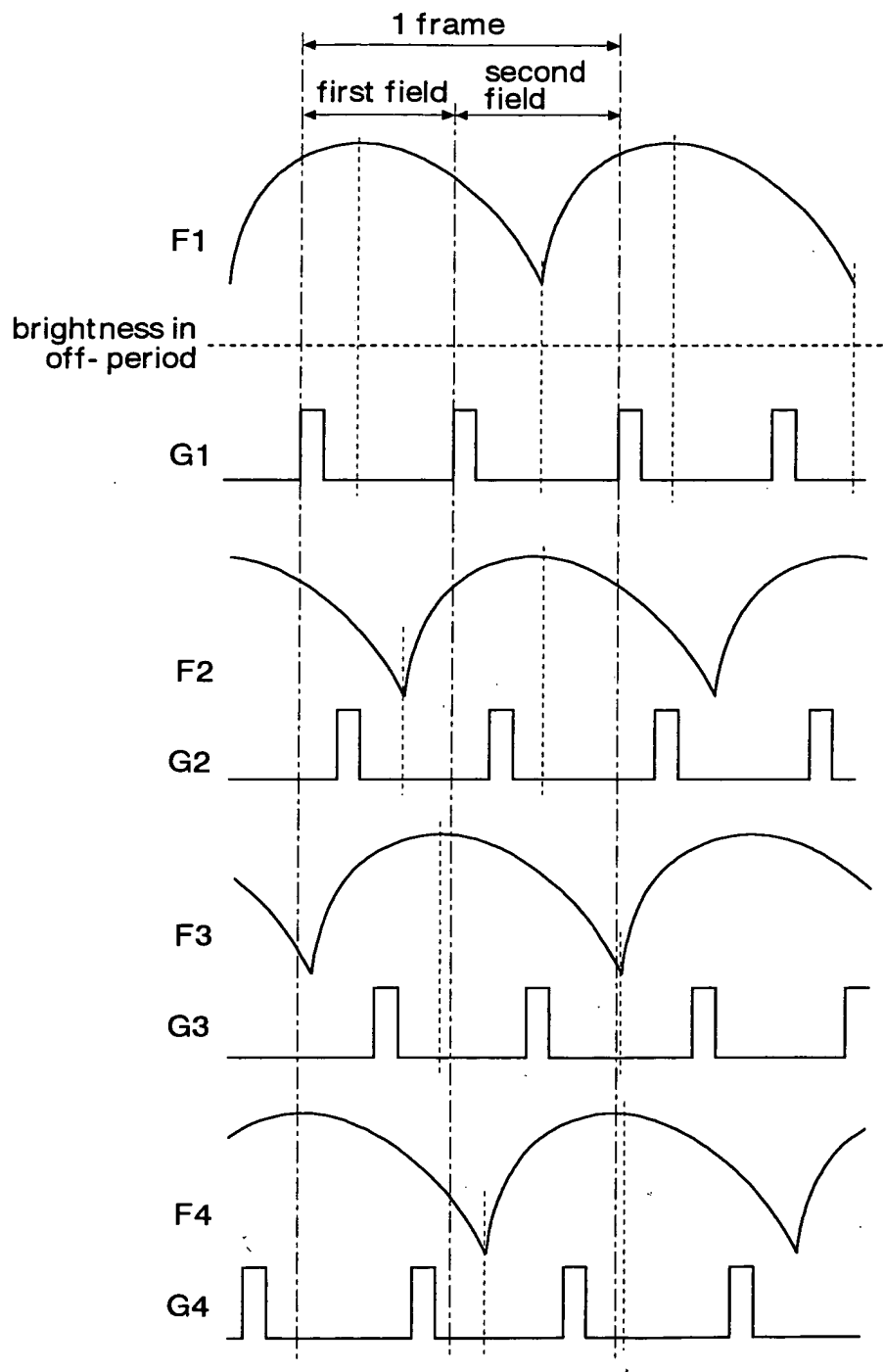


Fig. 20

The diagram illustrates the system architecture. At the top, 'display data' is input to a control block containing four sub-components: a control circuit (32), a hold driving circuit (34), an impulse driving circuit (36), and a gamma correction table (38). The control circuit (32) outputs a signal to a Y driver (14). The hold driving circuit (34) outputs a signal to an X driver (16). The impulse driving circuit (36) outputs a signal to the display panel. The gamma correction table (38) outputs a signal to the display panel. The X driver (16) is connected to four columns of the display panel, labeled D1, D2, D3, and D4. The Y driver (14) is connected to four rows of the display panel, labeled G1, G2, G3, and G4. The display panel is a grid of cells, with some cells shaded to represent fluorescent tubes. A temperature detection signal is shown as an input to the impulse driving circuit (36) and the display panel. The display panel is connected to four fluorescent tubes, labeled F1, F2, F3, and F4.

**Fig. 21**

09651288.083000

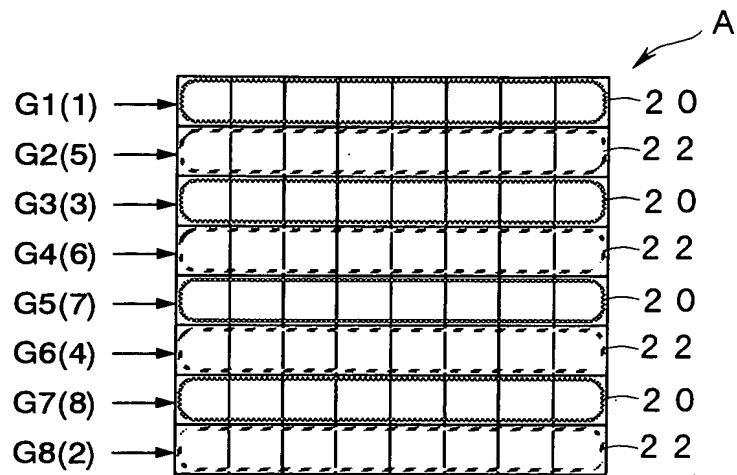


Fig. 22

**Fig. 23**

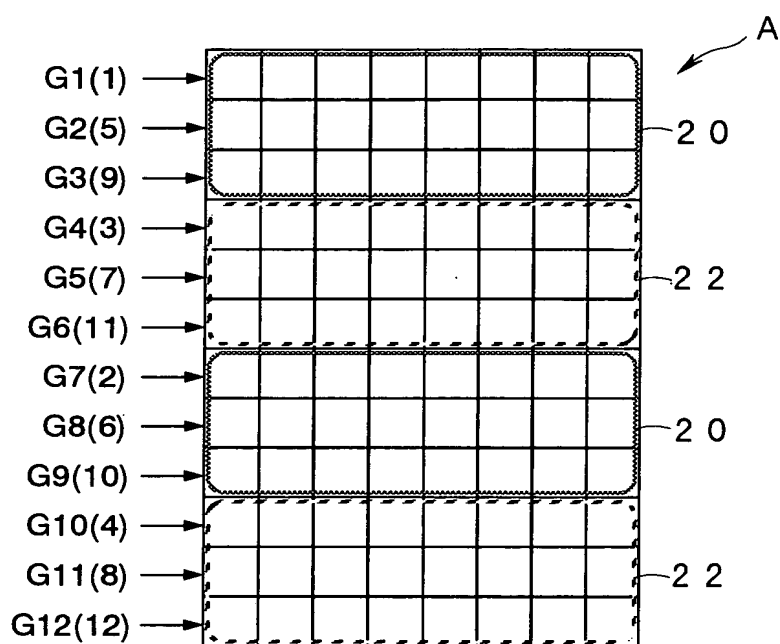


Fig. 24





fluorescent tube

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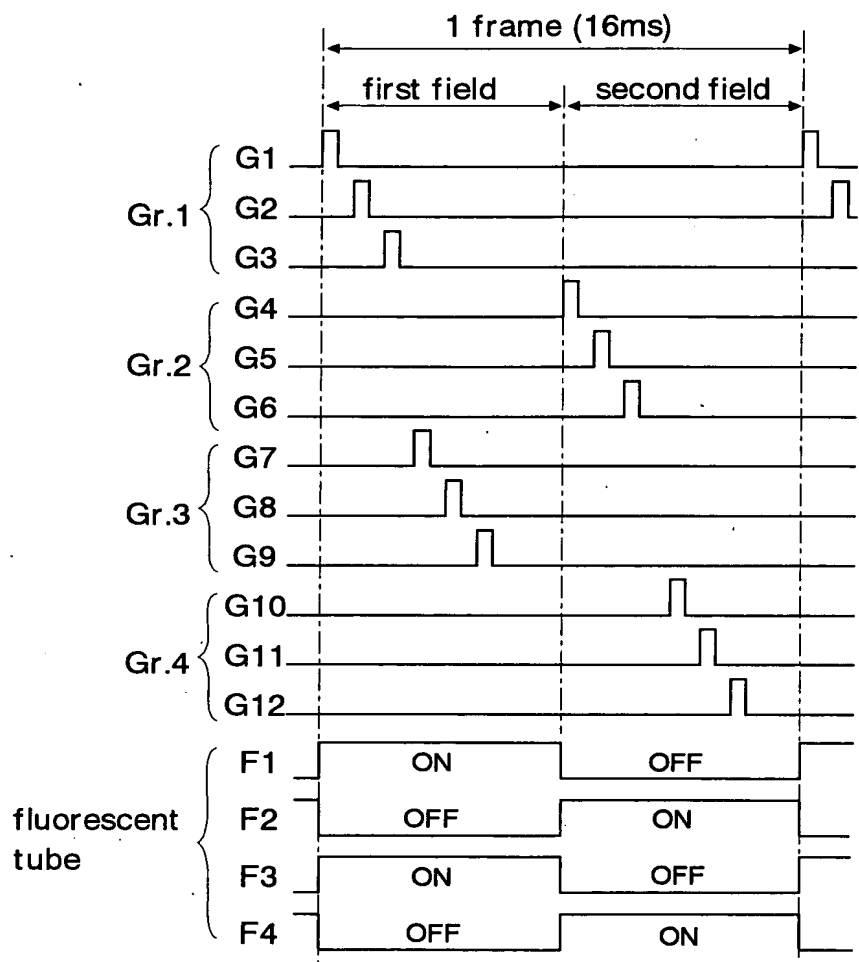


Fig. 27

fluorescent tube

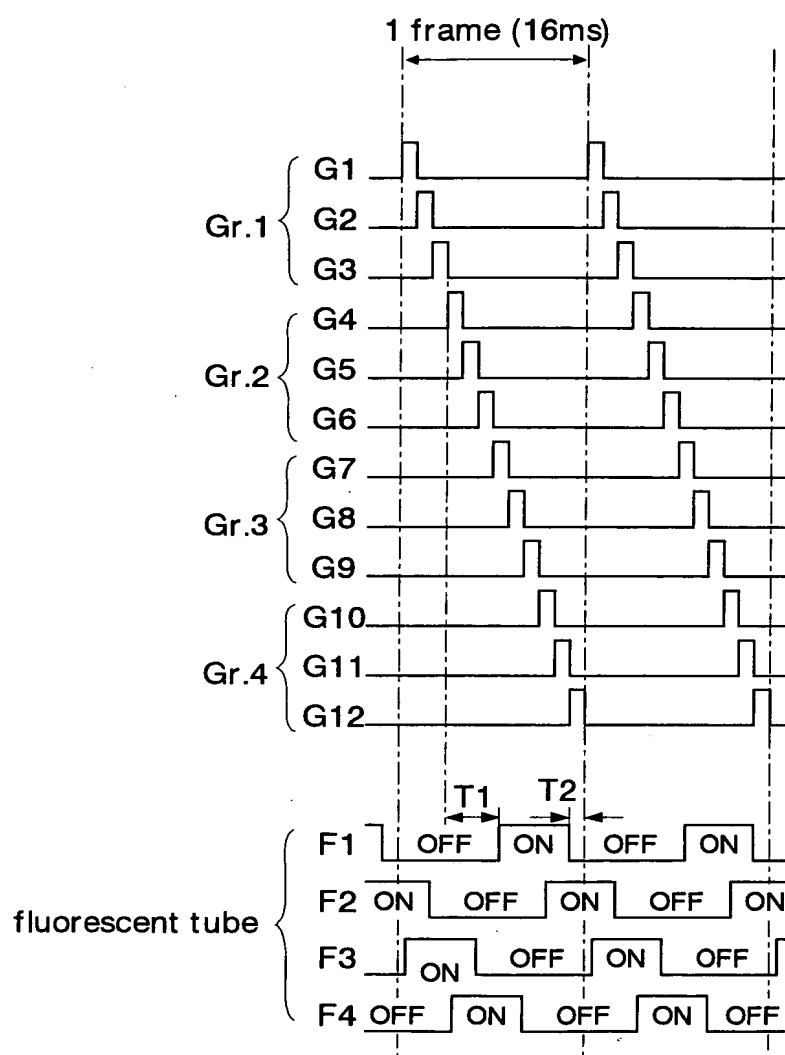


Fig. 29

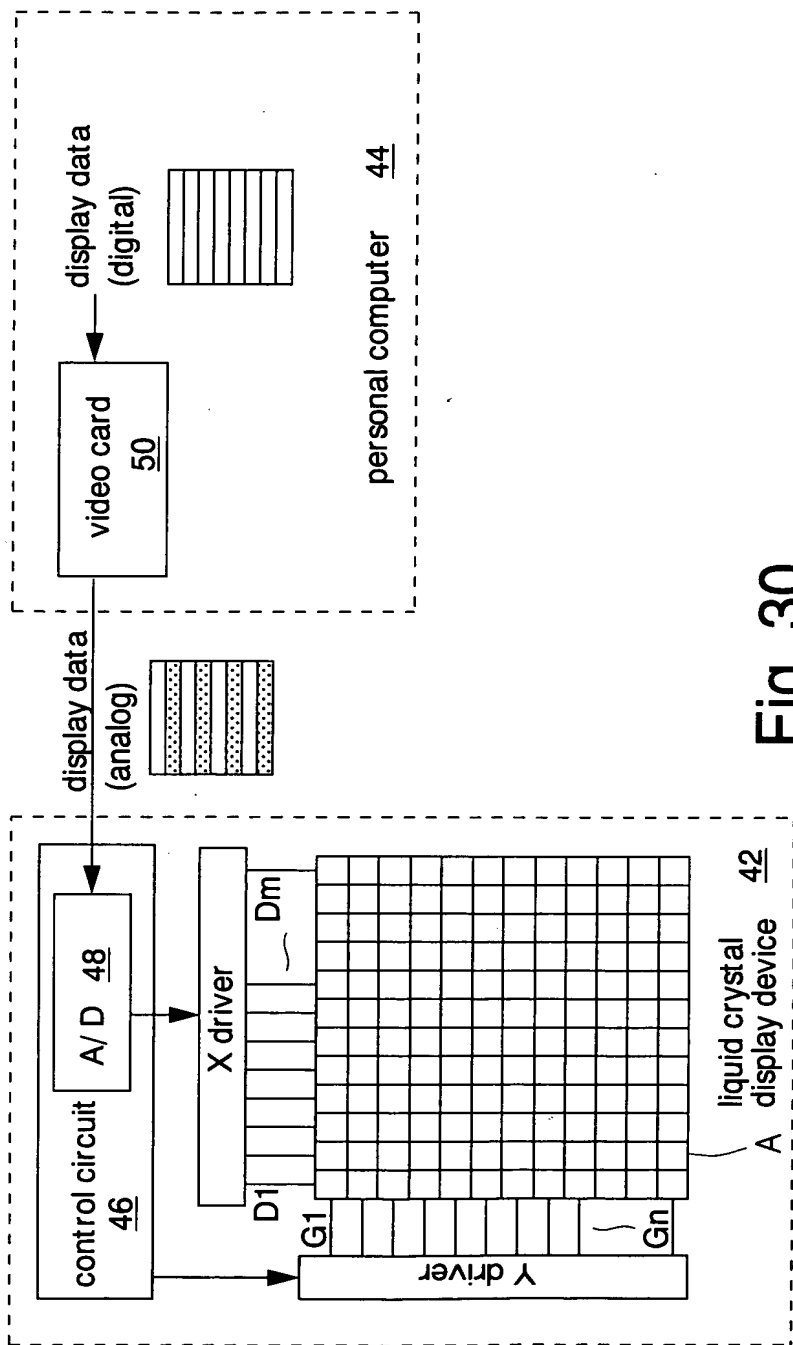


Fig. 30

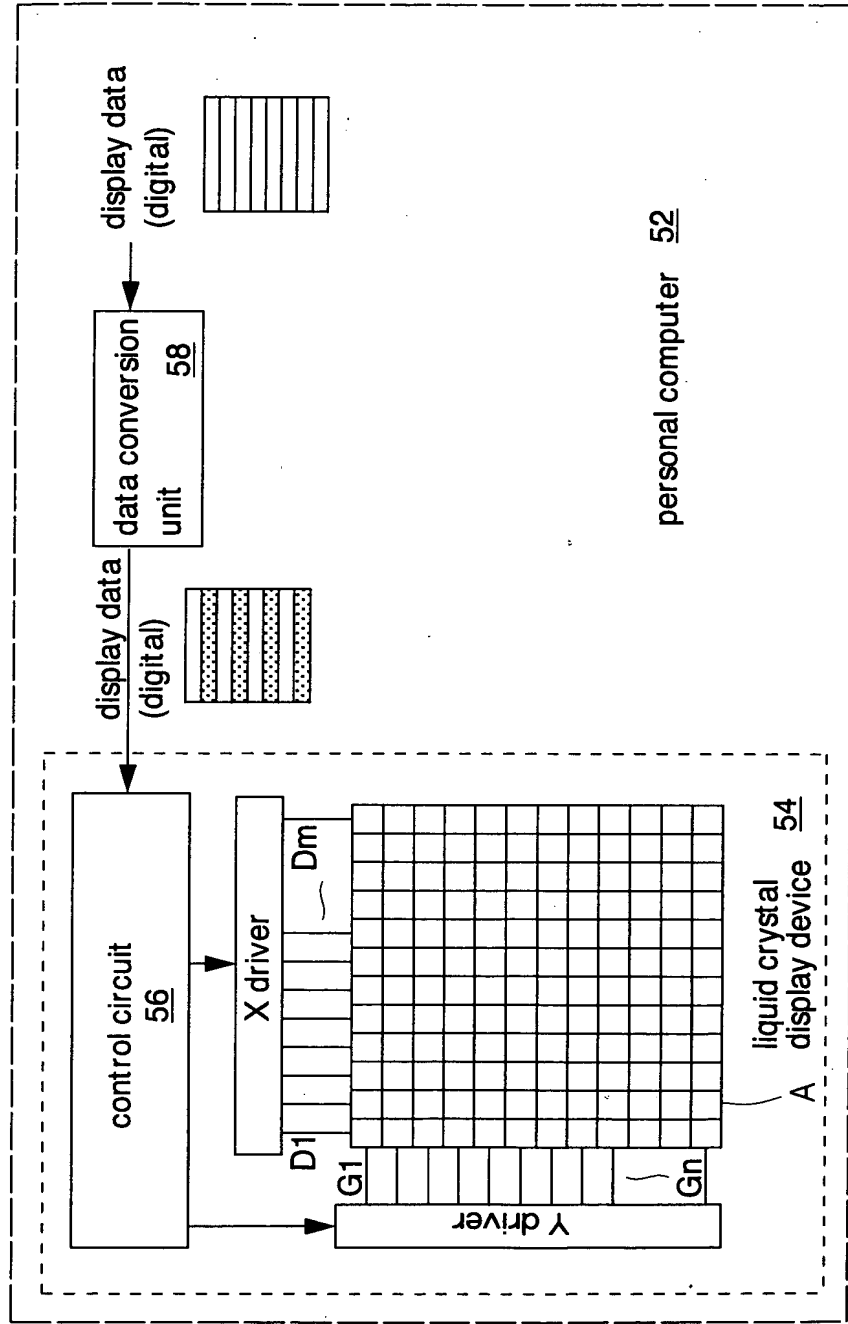


Fig. 31

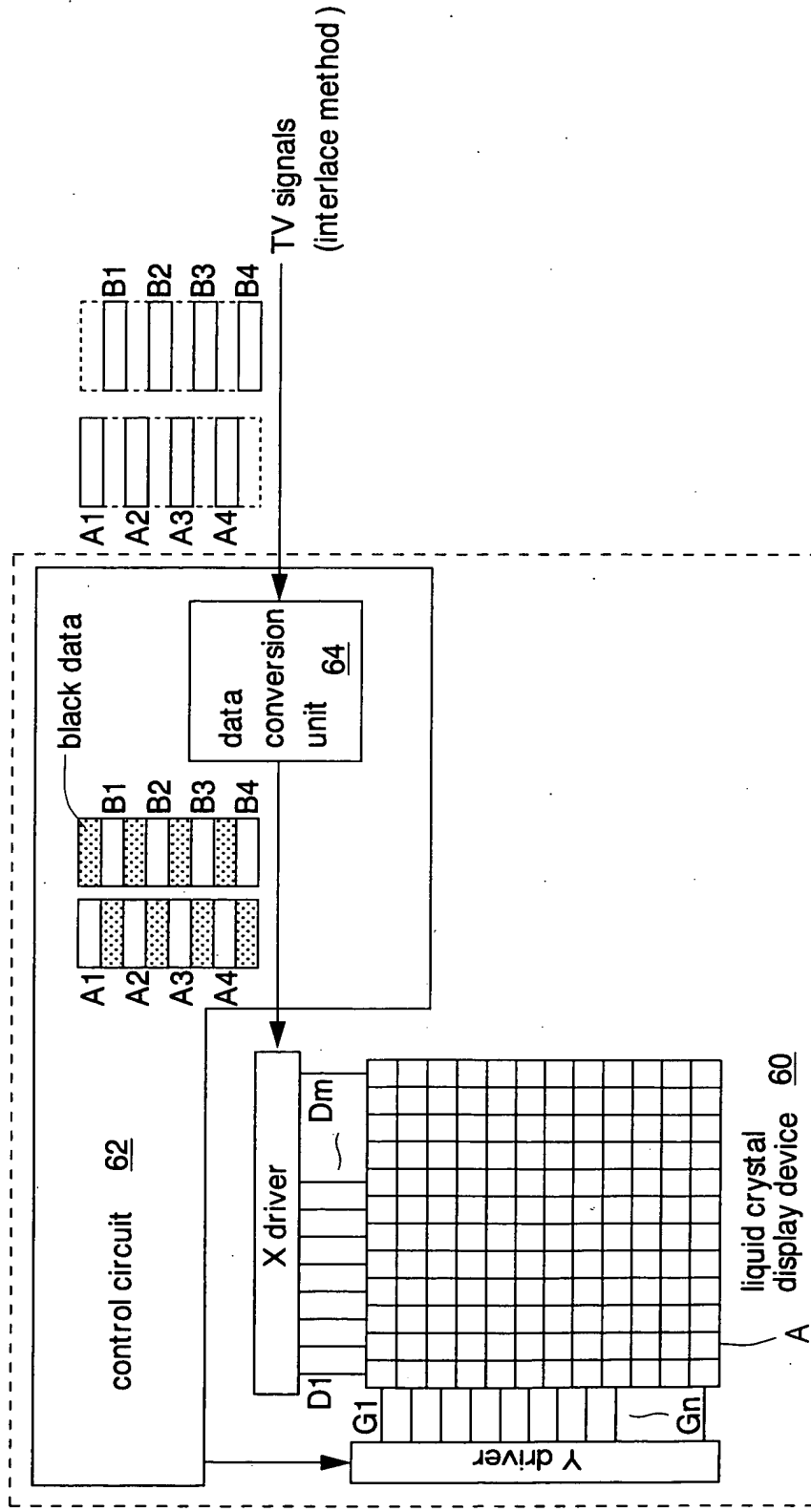
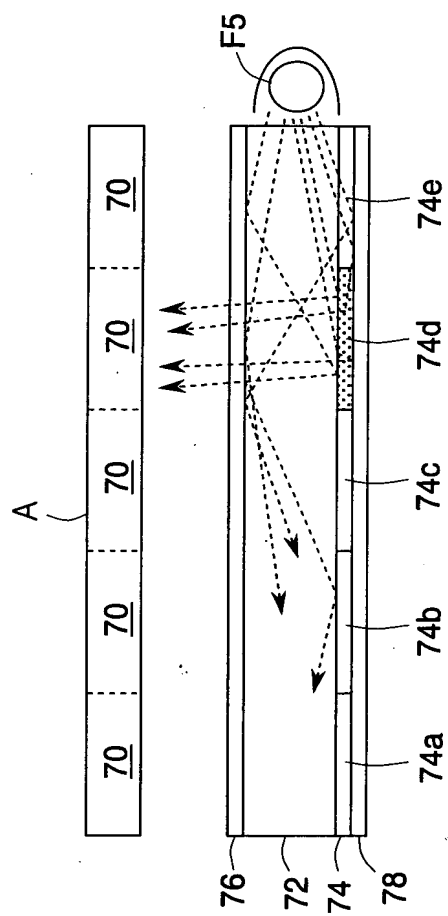


Fig. 32



**Fig. 33**



**Fig. 34**

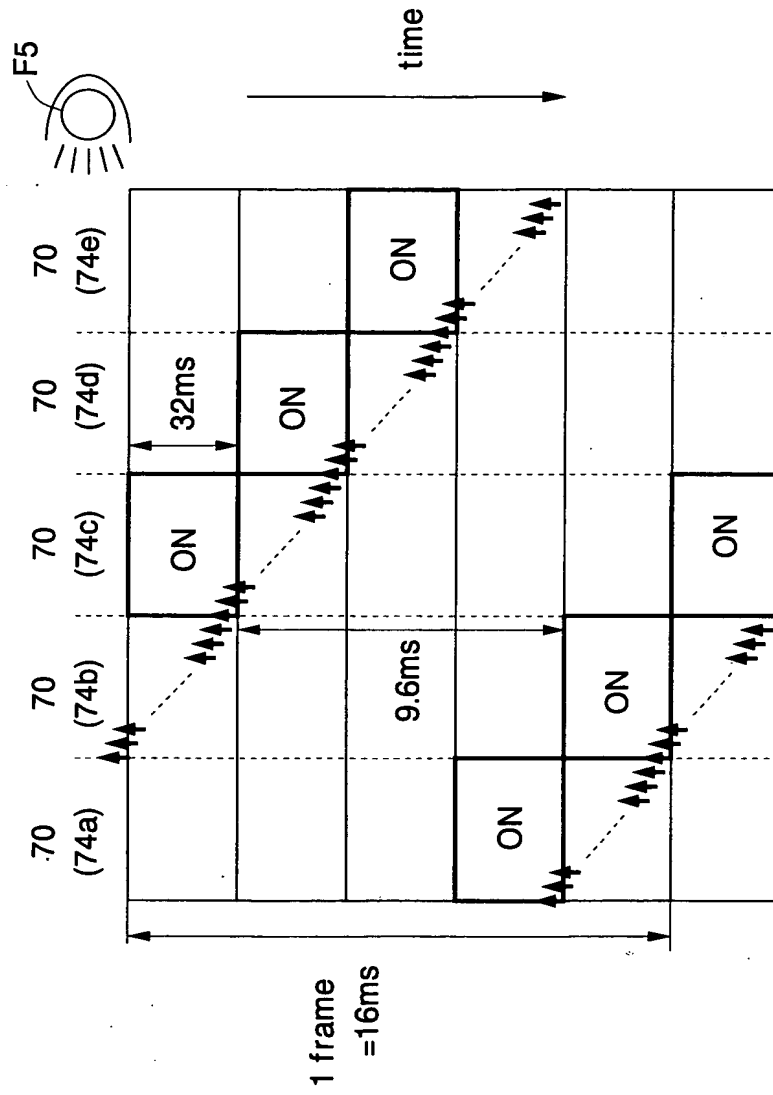
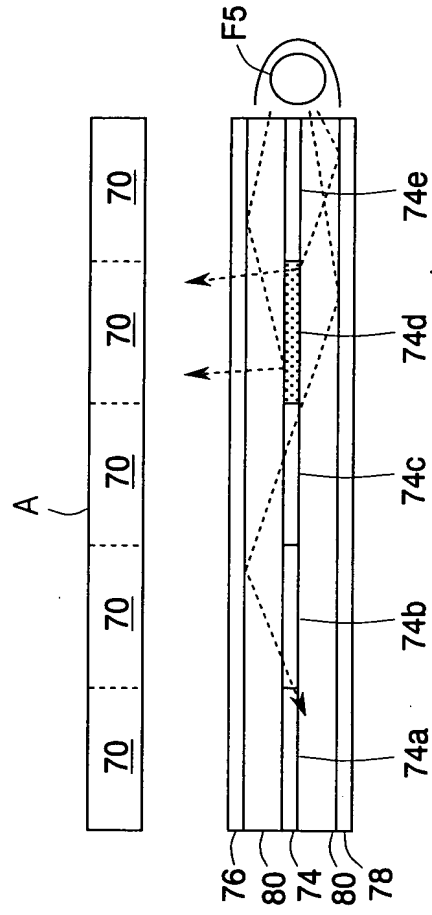


Fig. 35



**Fig. 36**



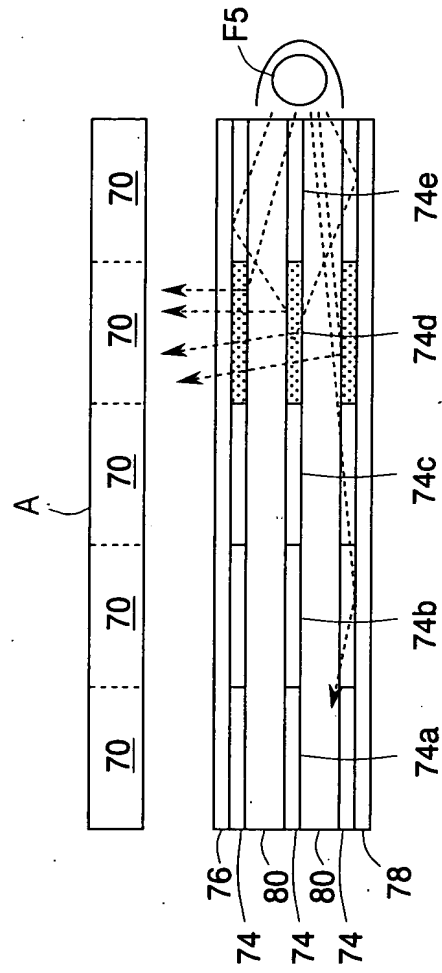


Fig. 38

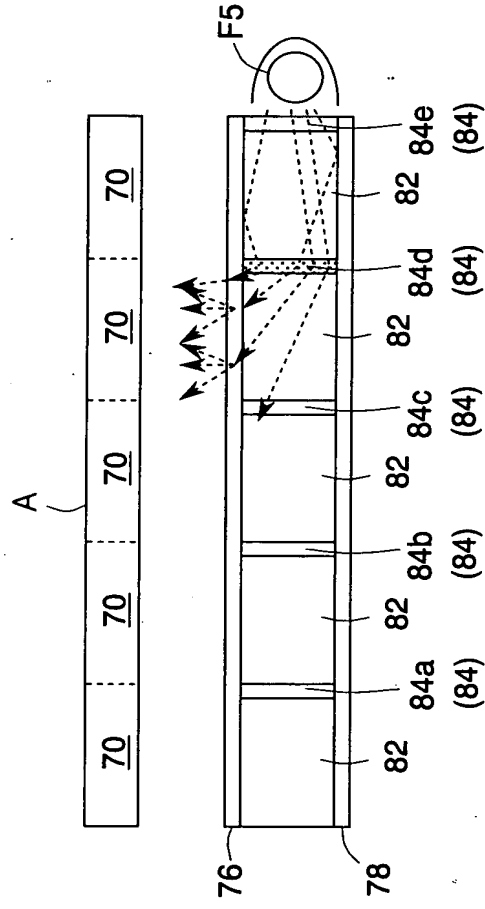


Fig. 39

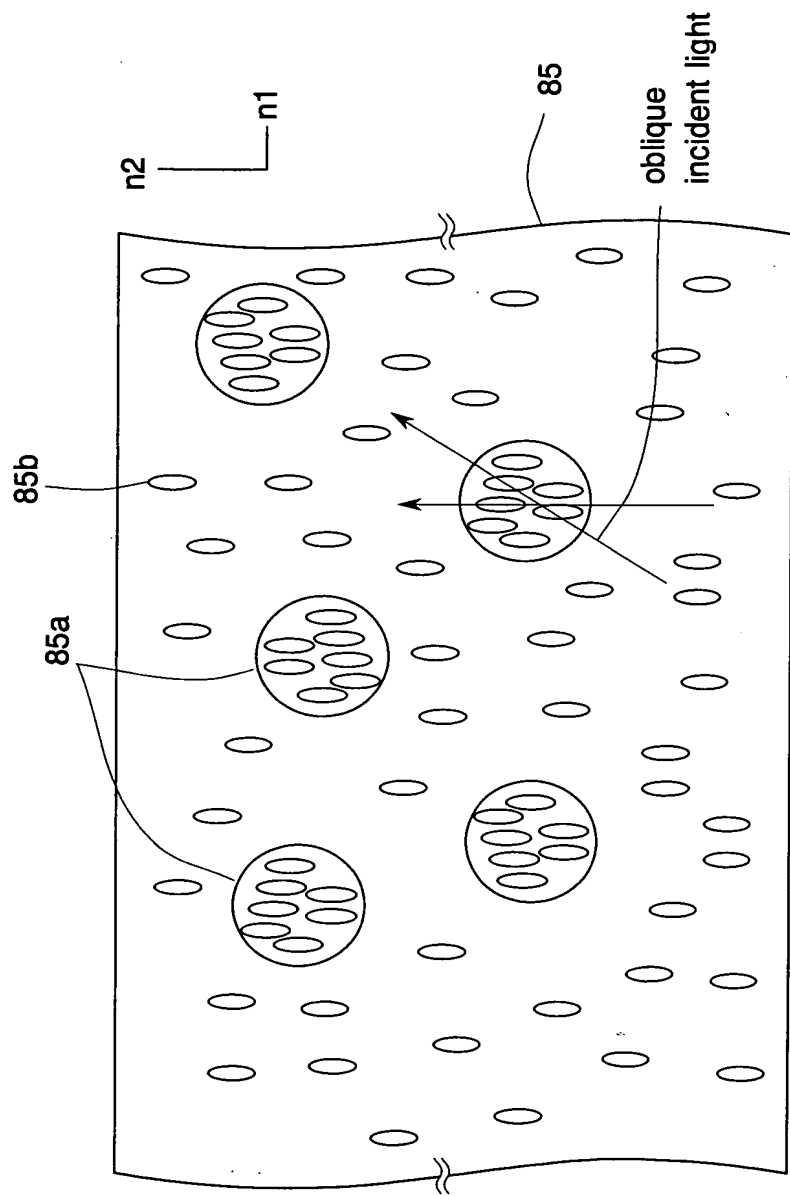
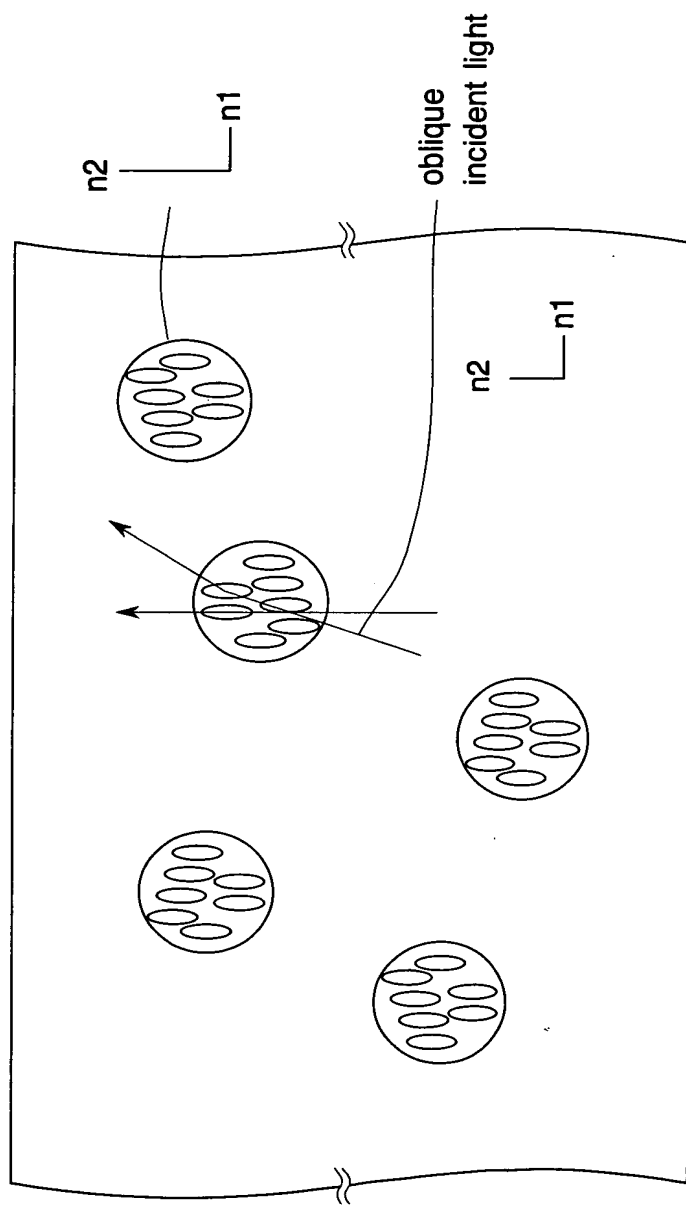


Fig. 40





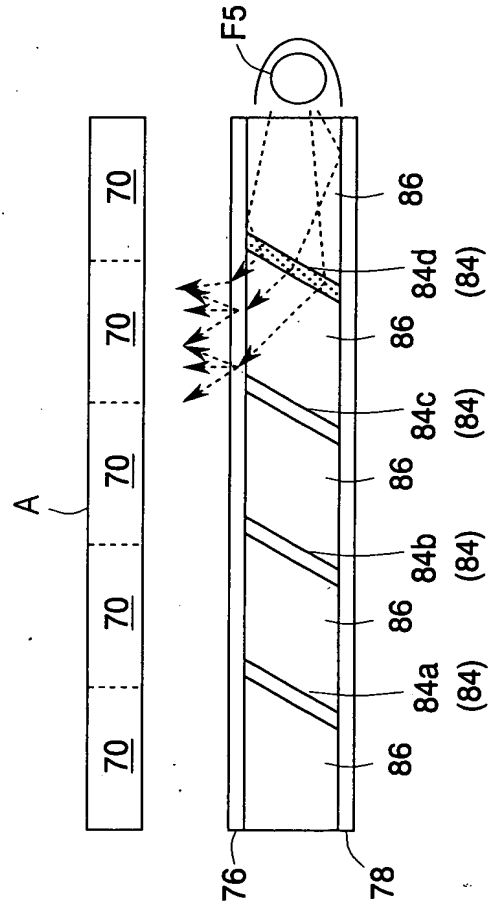
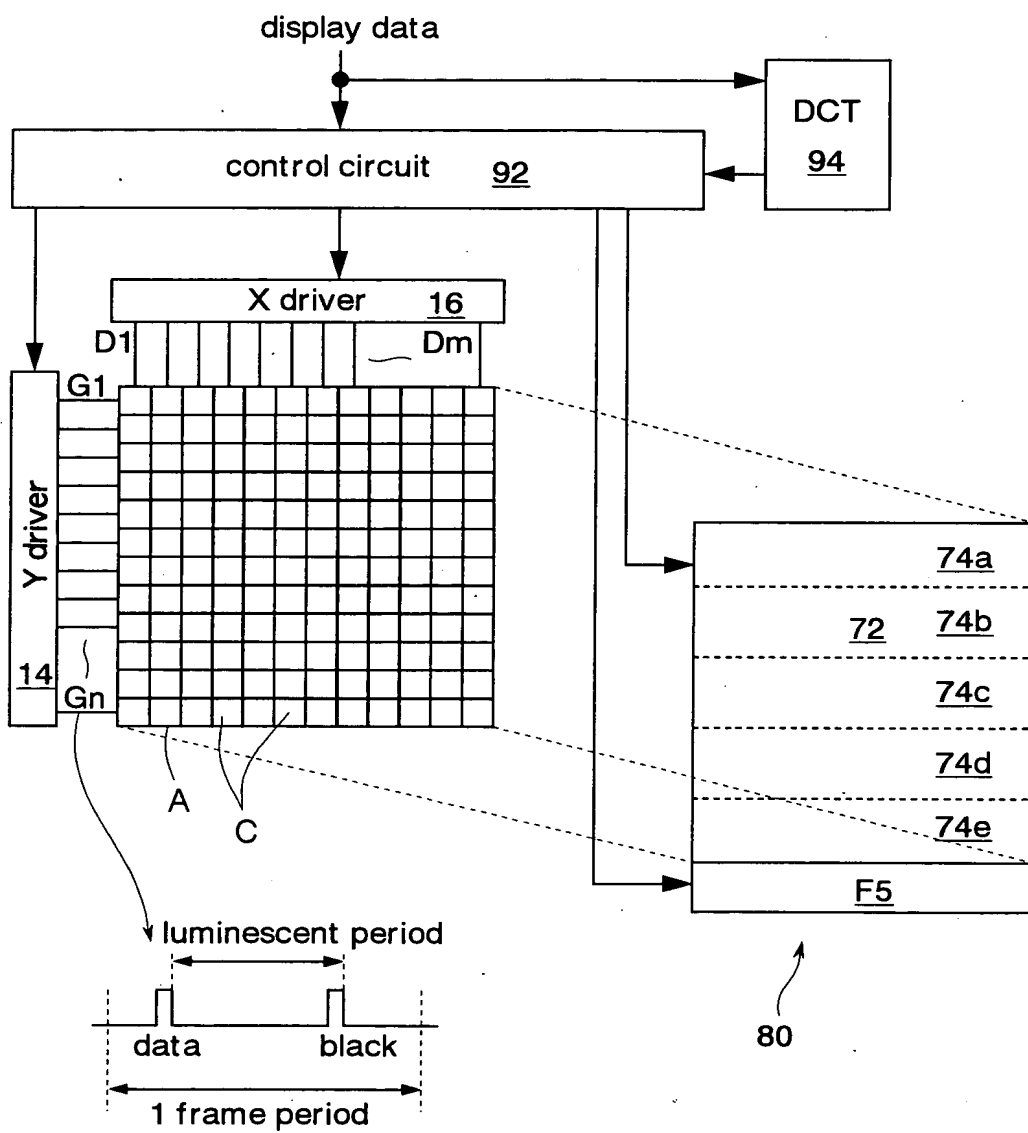


Fig. 42

**Fig. 43**



**Fig. 44**

80

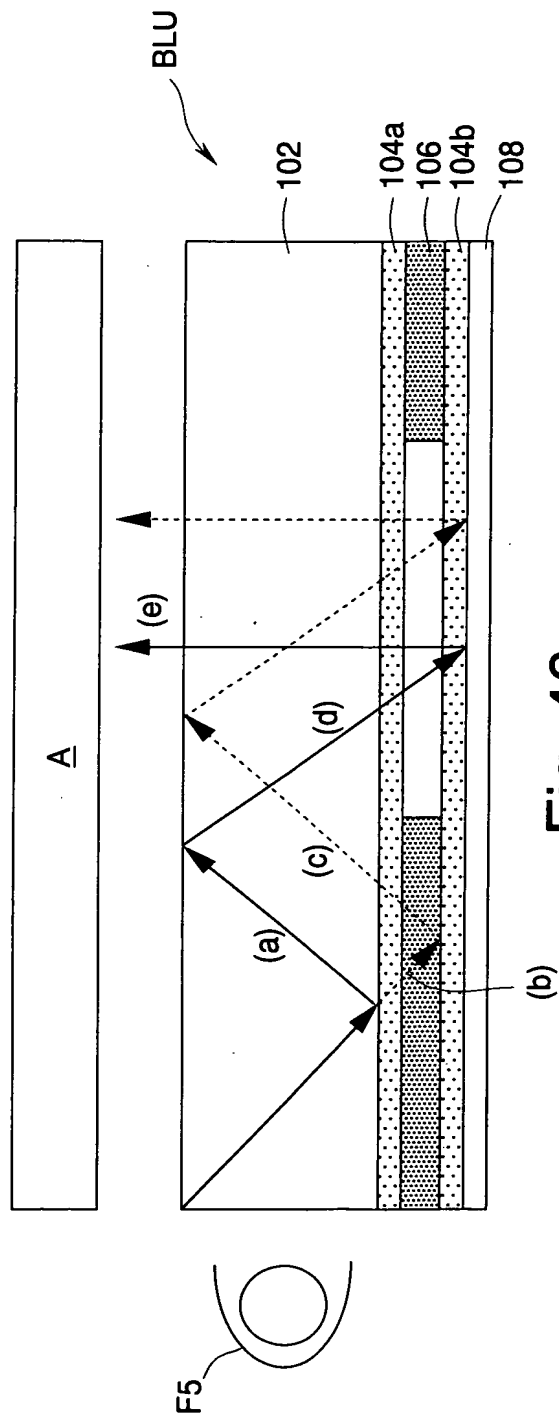


Fig. 46



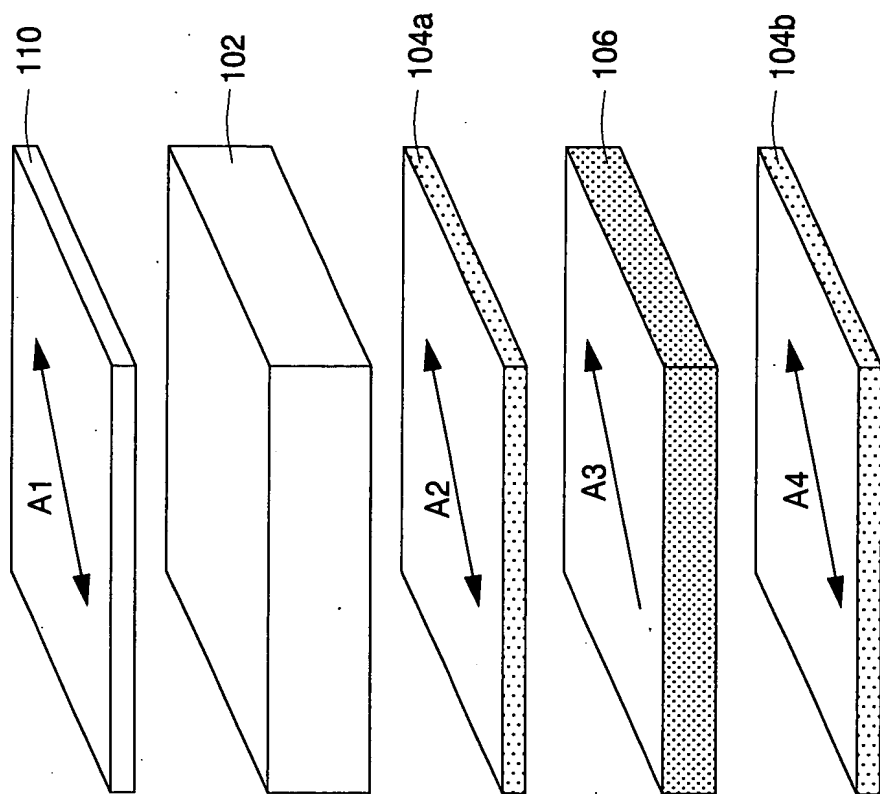


Fig. 48



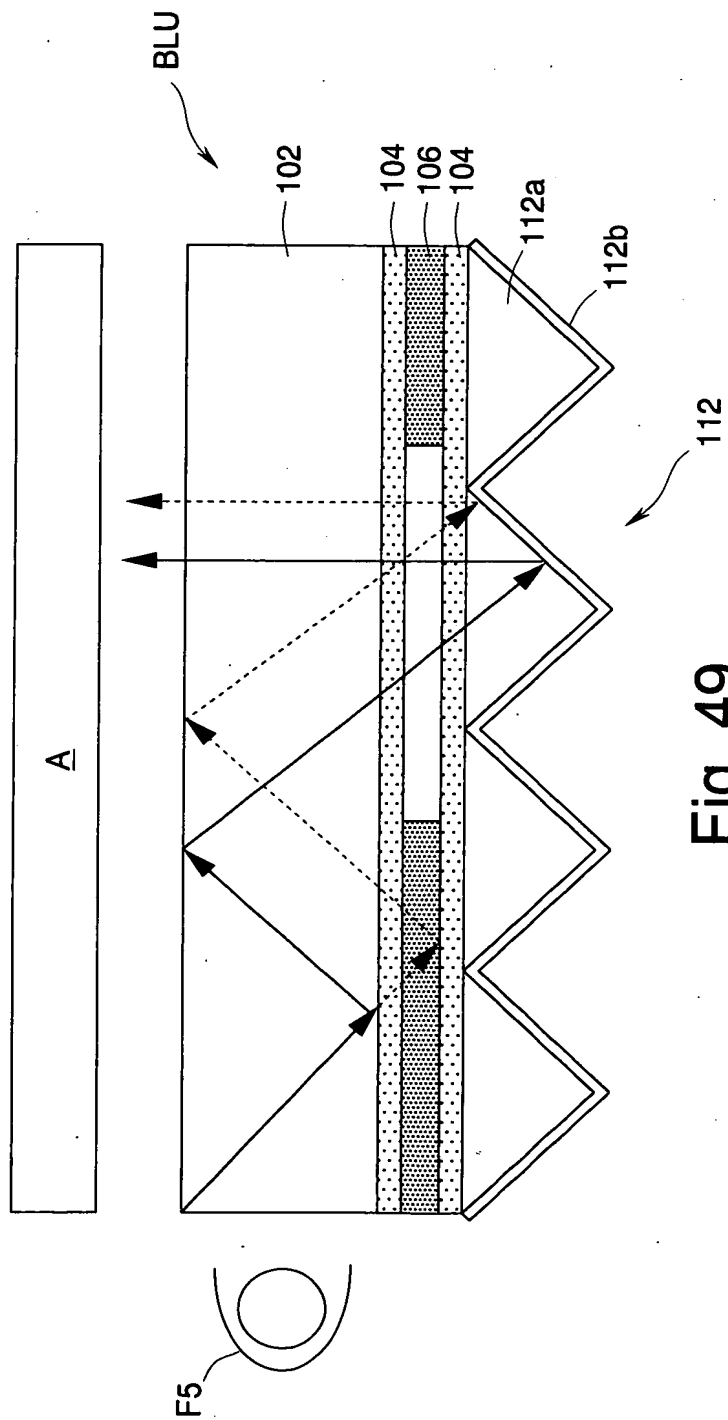


Fig. 49

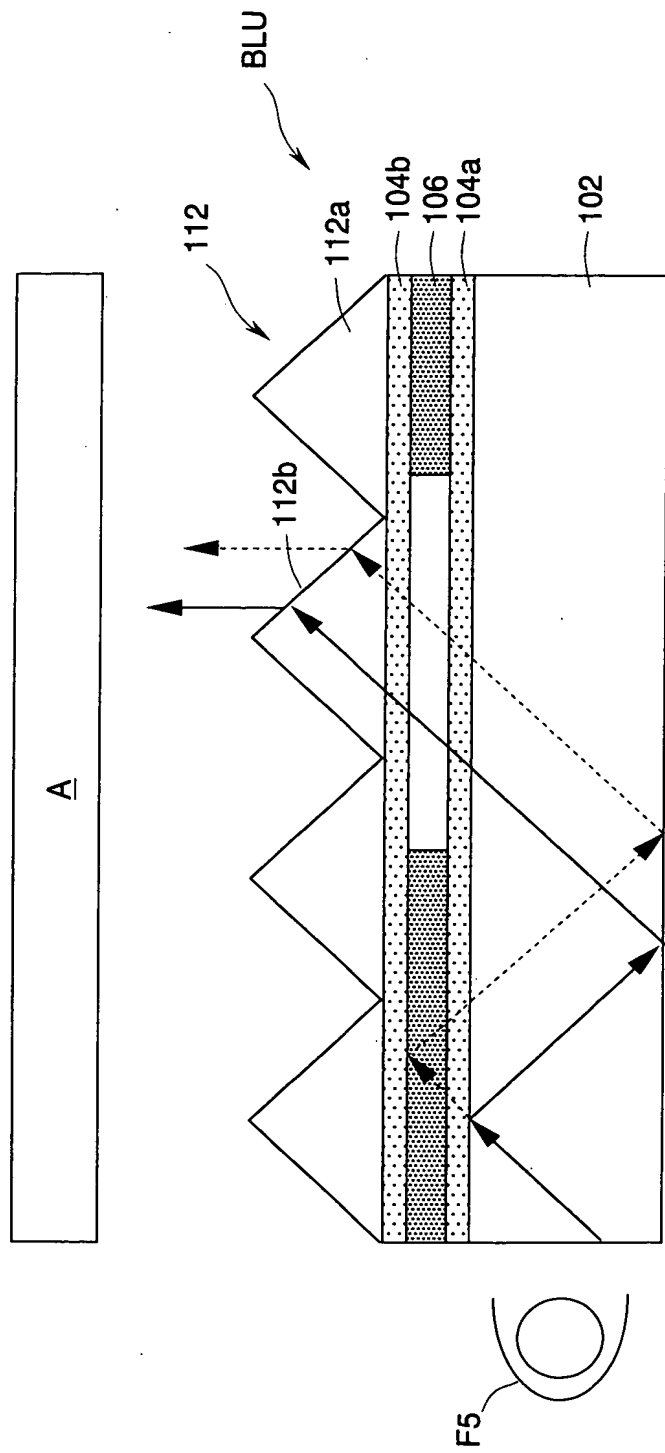


Fig. 50

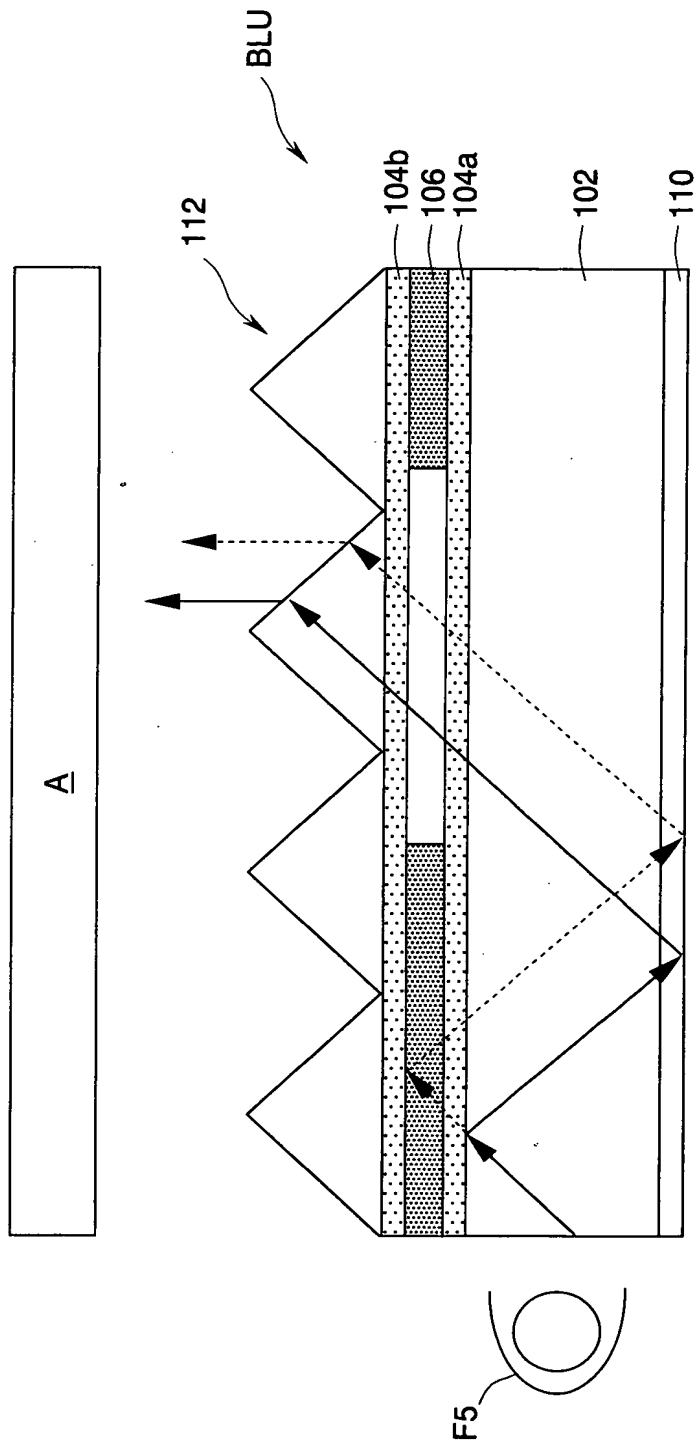


Fig. 51



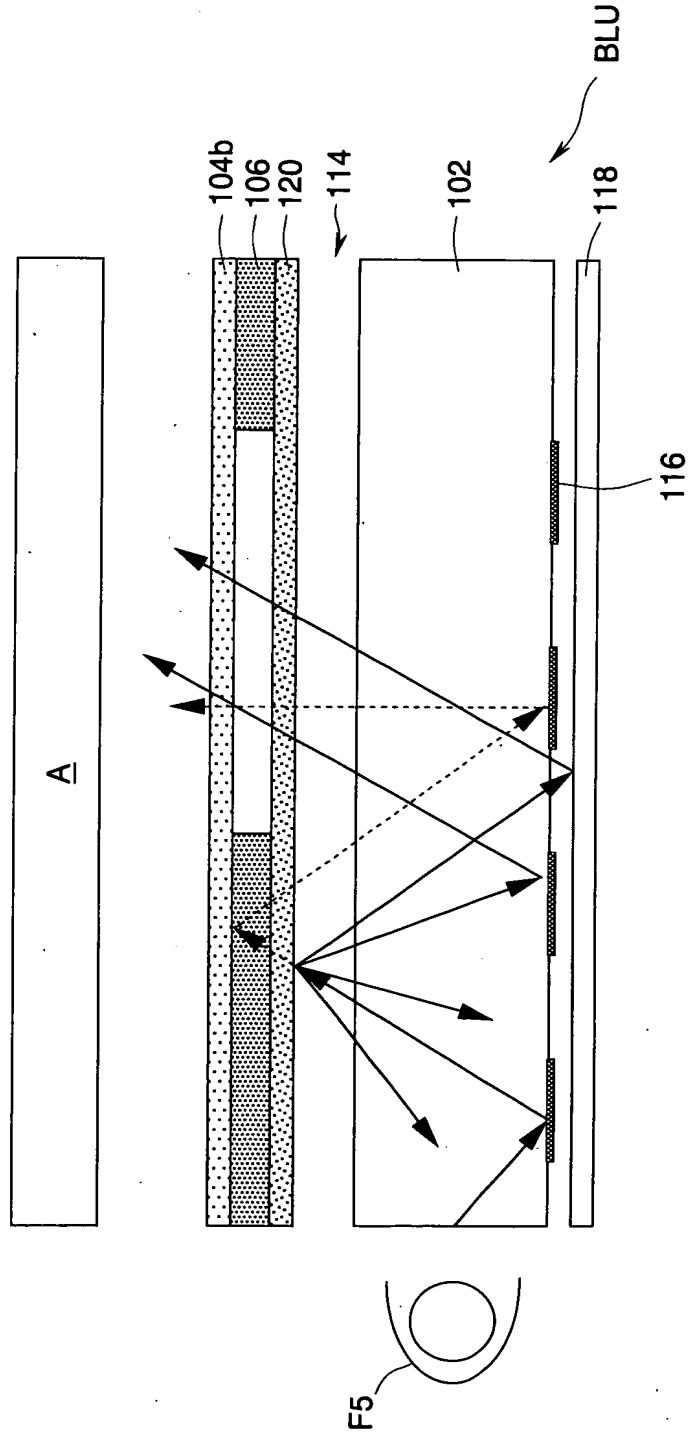


Fig. 53

**Fig. 54**

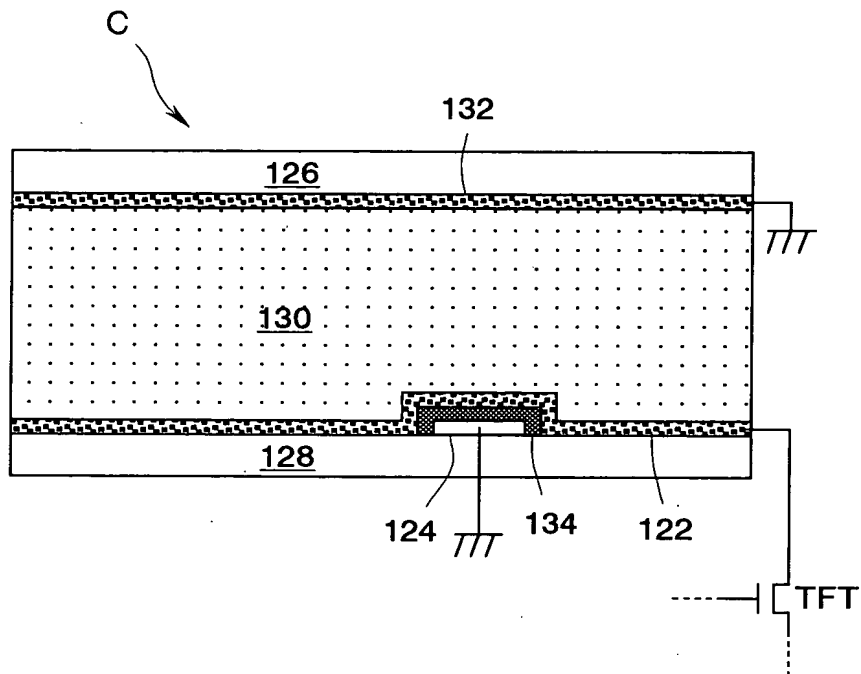


Fig. 55

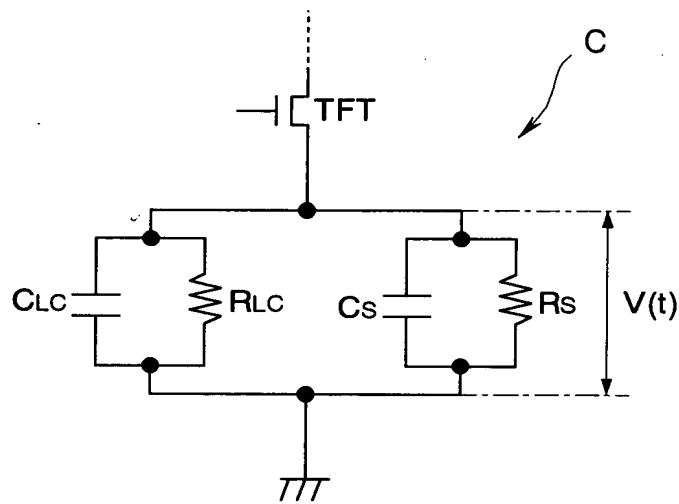


Fig. 56



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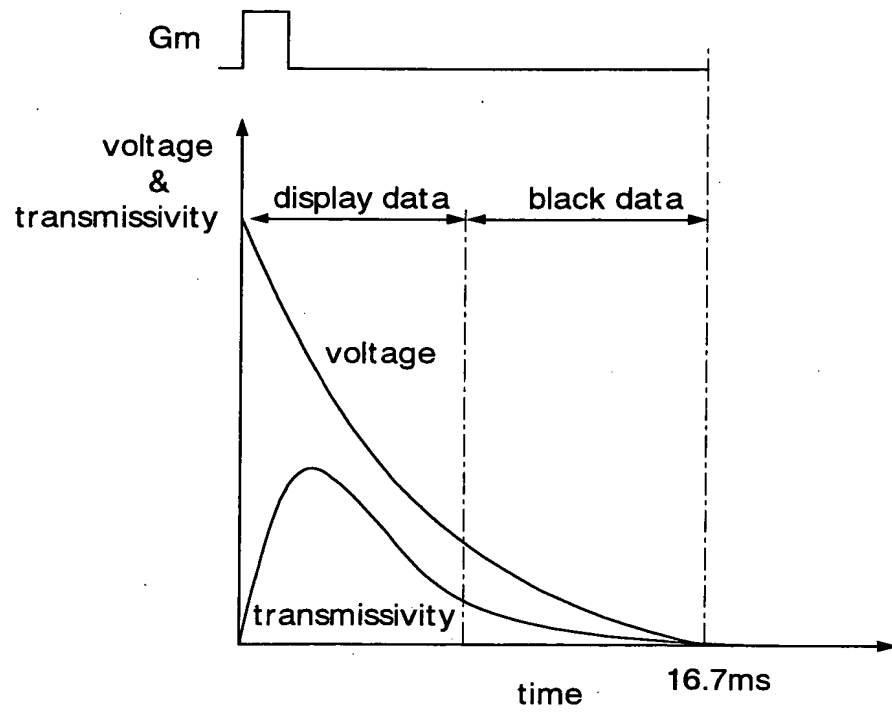


Fig. 57

The graph shows the voltage  $V(t)$  in percent on the y-axis (0 to 100) versus time in milliseconds on the x-axis (0 to 20). Several exponential decay curves are plotted for different time constants: 1.0, 0.1, 0.05, 0.01, 0.005, and 0.001 ms. A vertical dashed line at 16.7 ms indicates the time required for the voltage to decay to 10% for the 0.01 ms time constant curve.

**Fig. 58**

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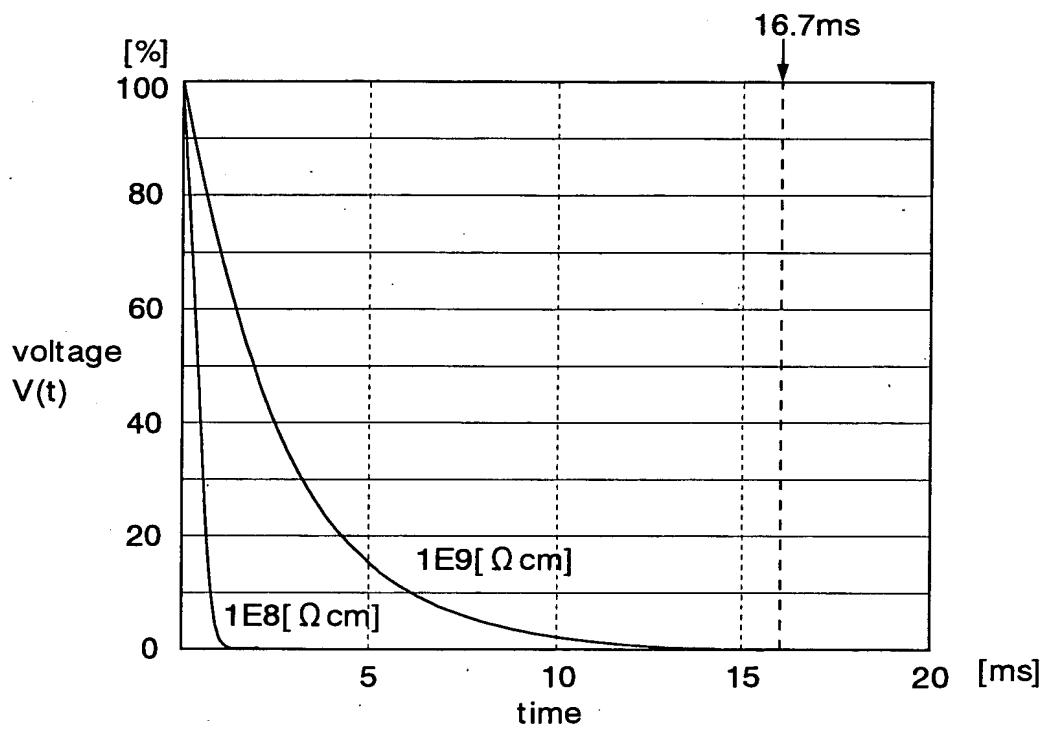


Fig. 59

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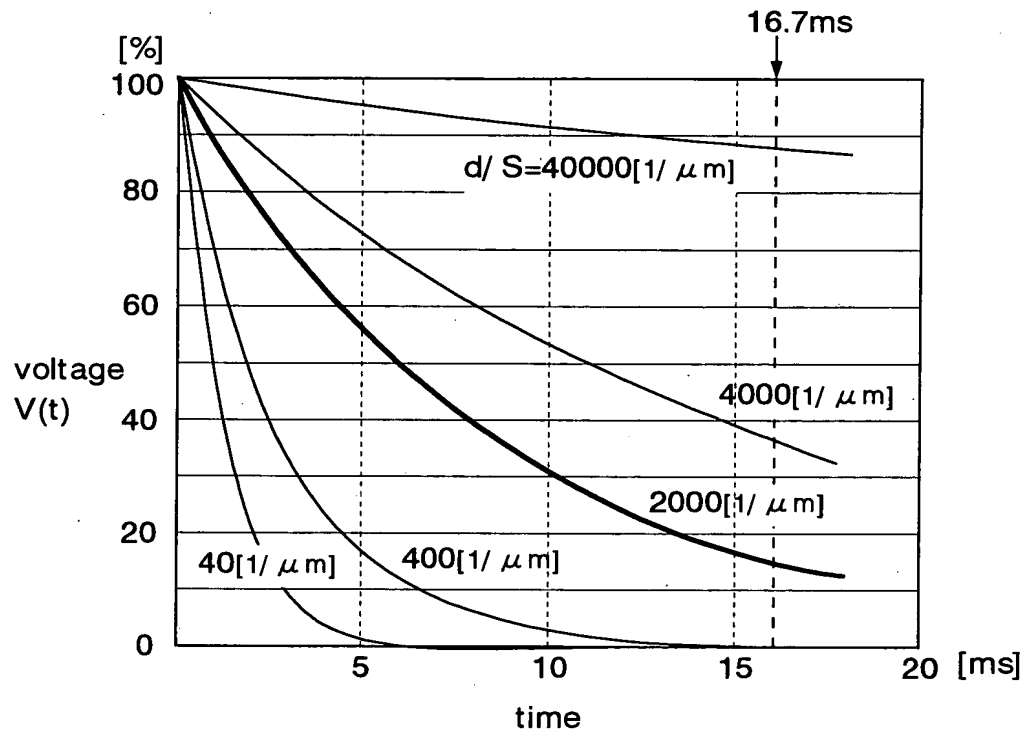


Fig. 60

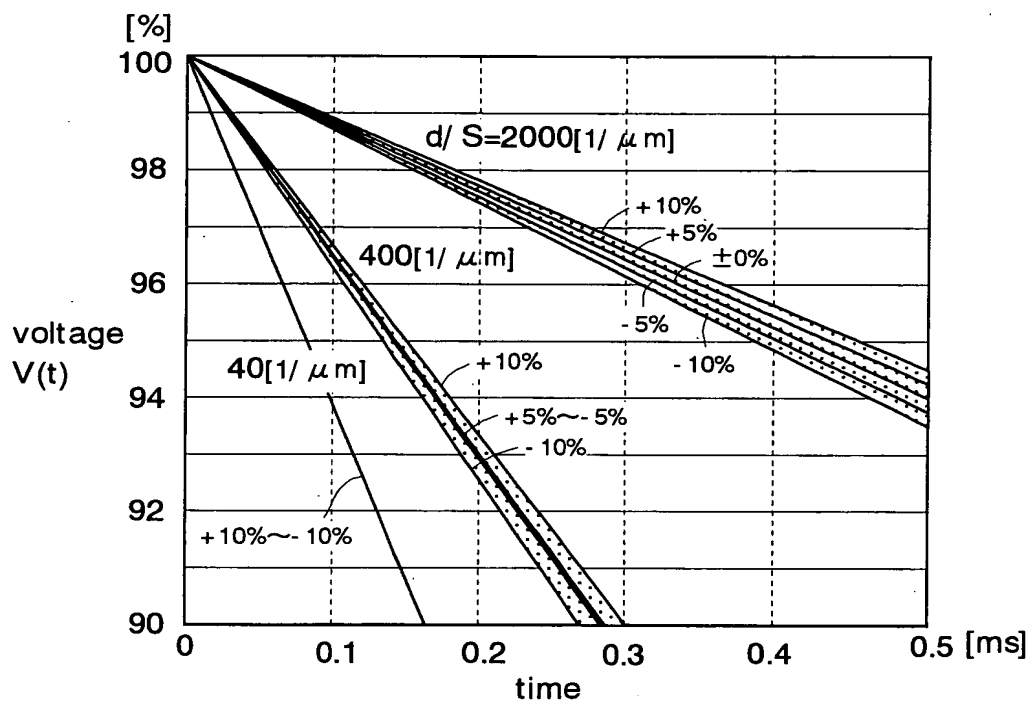
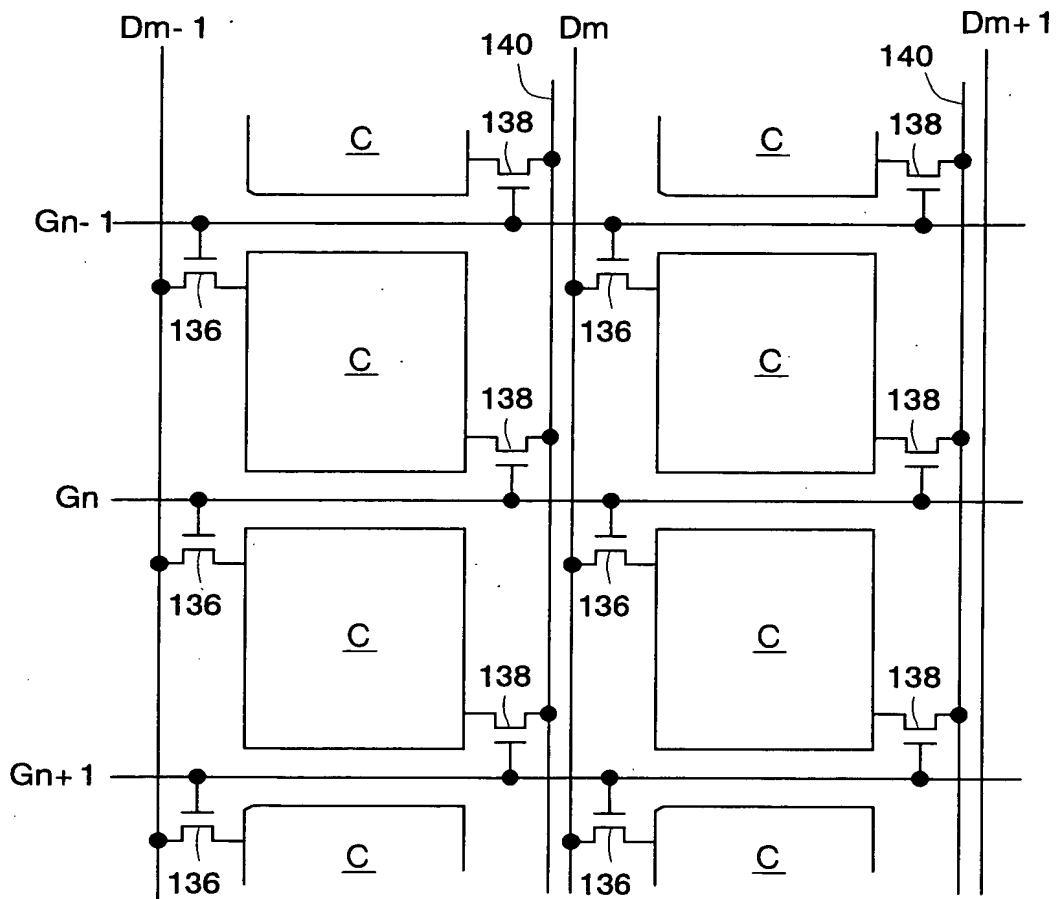


Fig. 61



**Fig. 62**

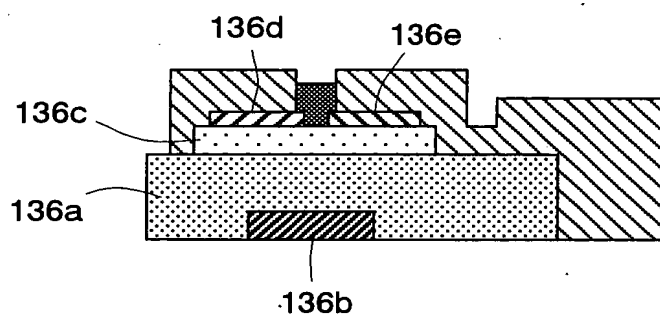
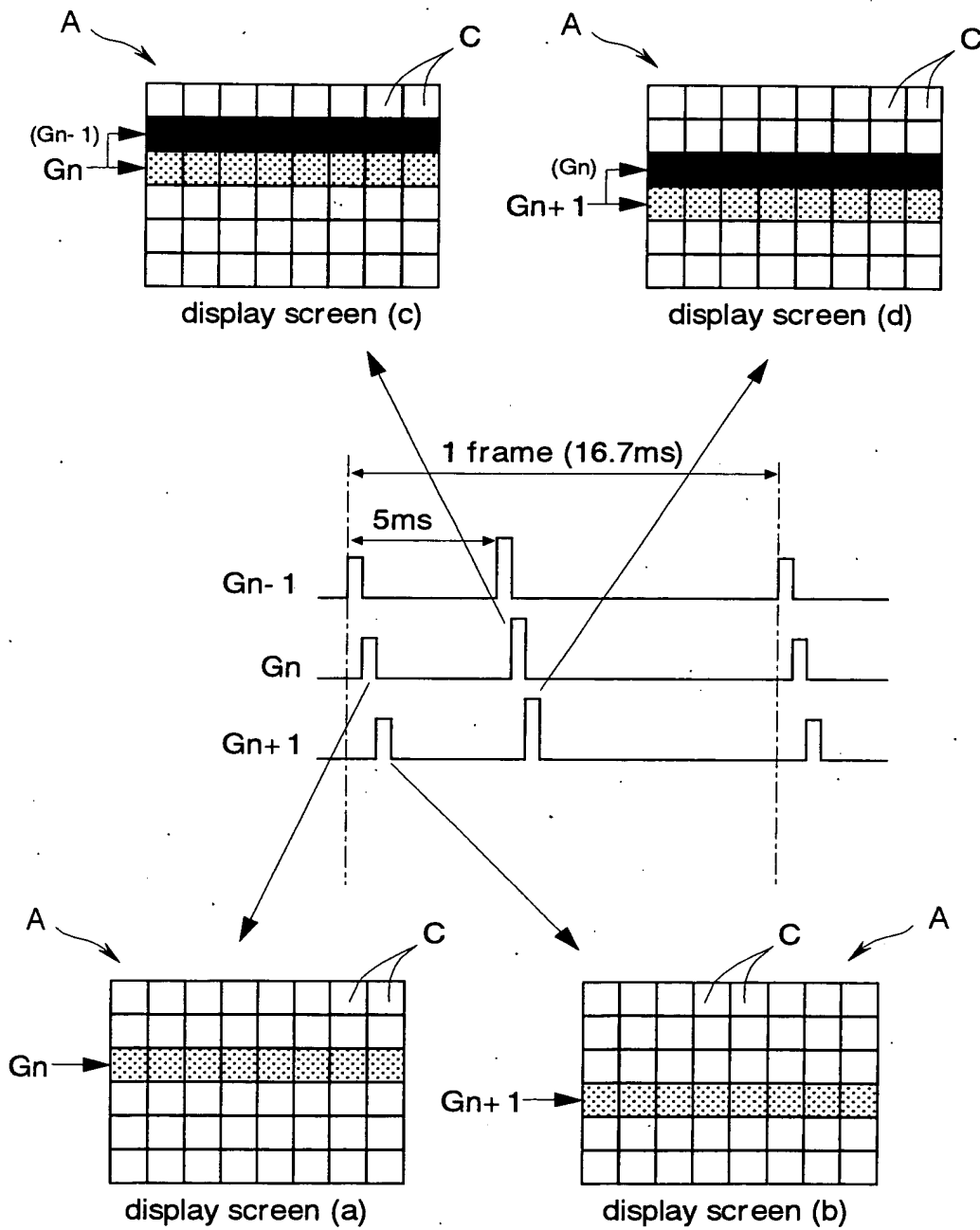


Fig. 63



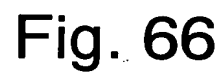
**Fig. 64**



The diagram illustrates a 2D array of memory cells. The columns are labeled  $Dm-1$ ,  $Dm$ , and  $Dm+1$ . The rows are labeled  $Gn-1$ ,  $Gn$ , and  $Gn+1$ . Each cell contains a capacitor  $C$ . Access transistors are labeled 136 and 138. Word lines are labeled 140. The diagram shows a grid of cells with access transistors connecting them to word lines and bit lines.

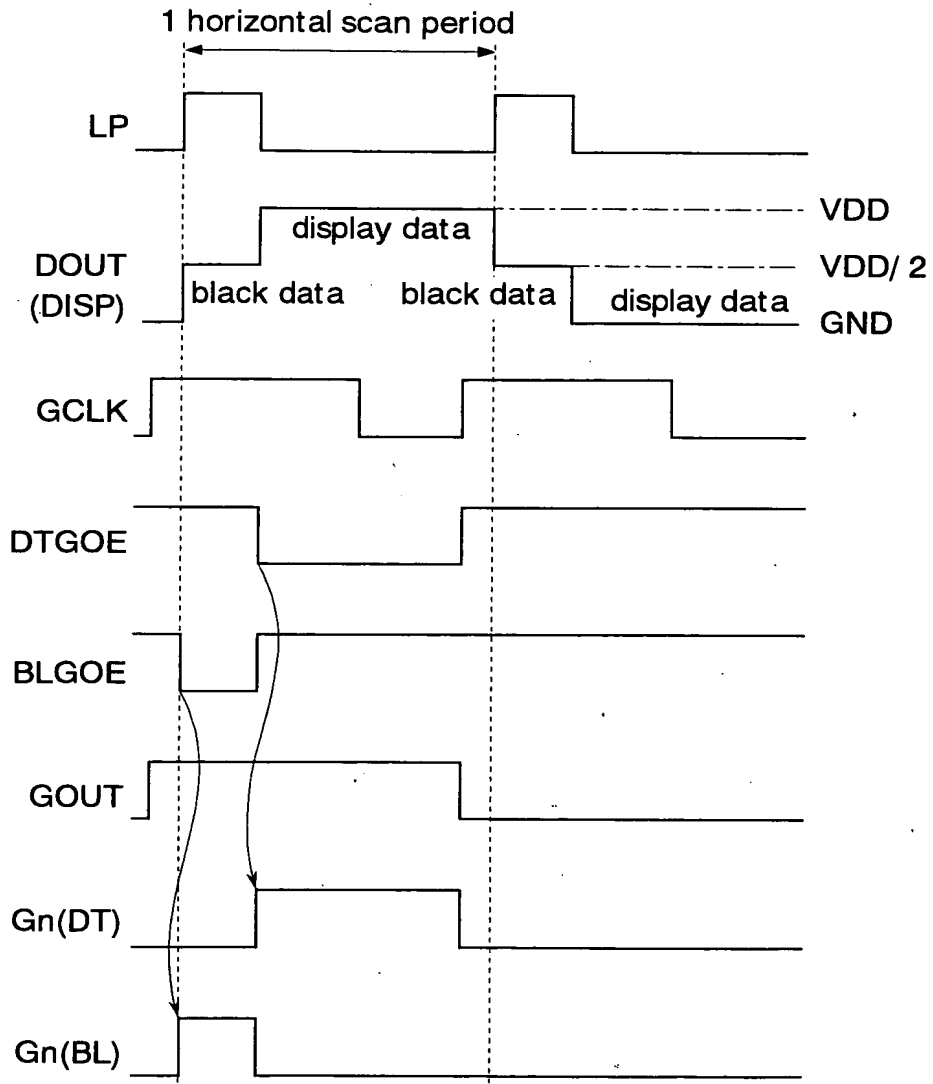
**Fig. 65**

DT BL



**Fig. 66**

**Fig. 67**



**Fig. 68**

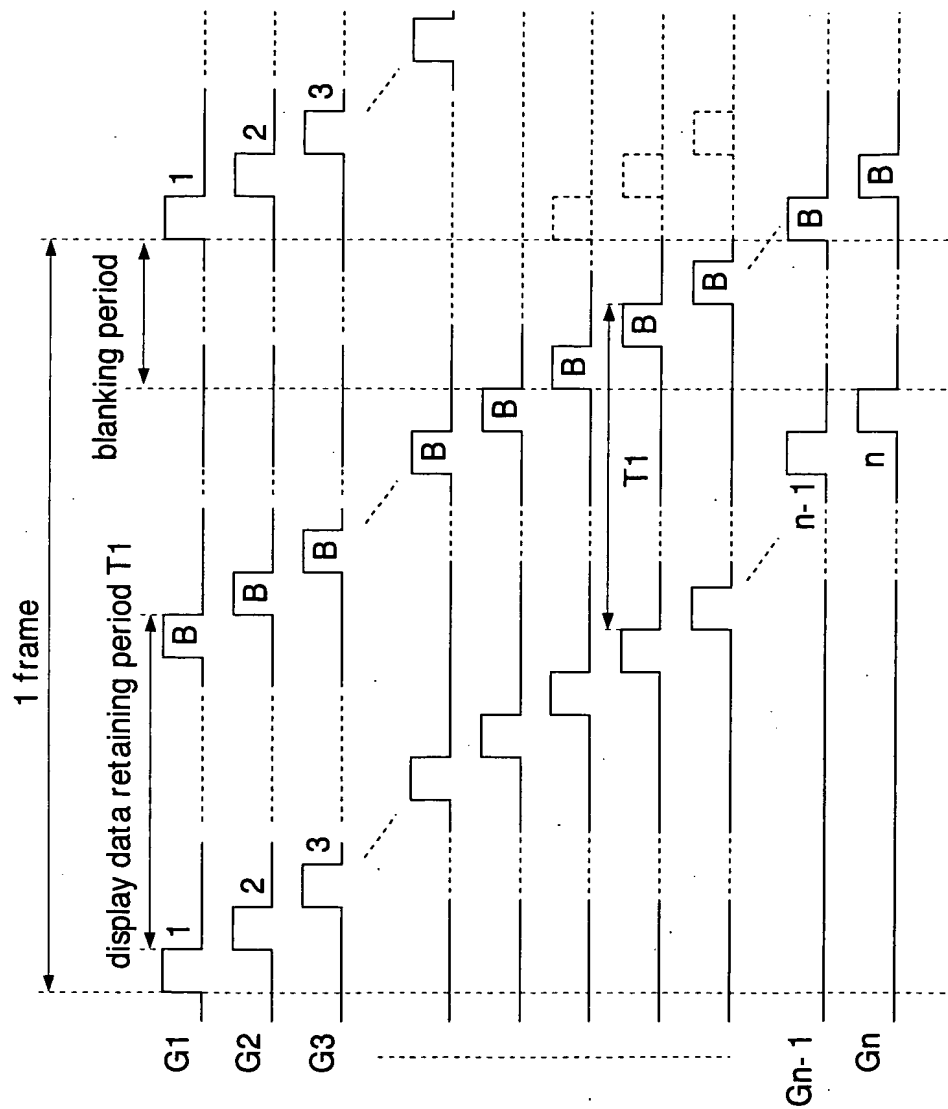


Fig. 69

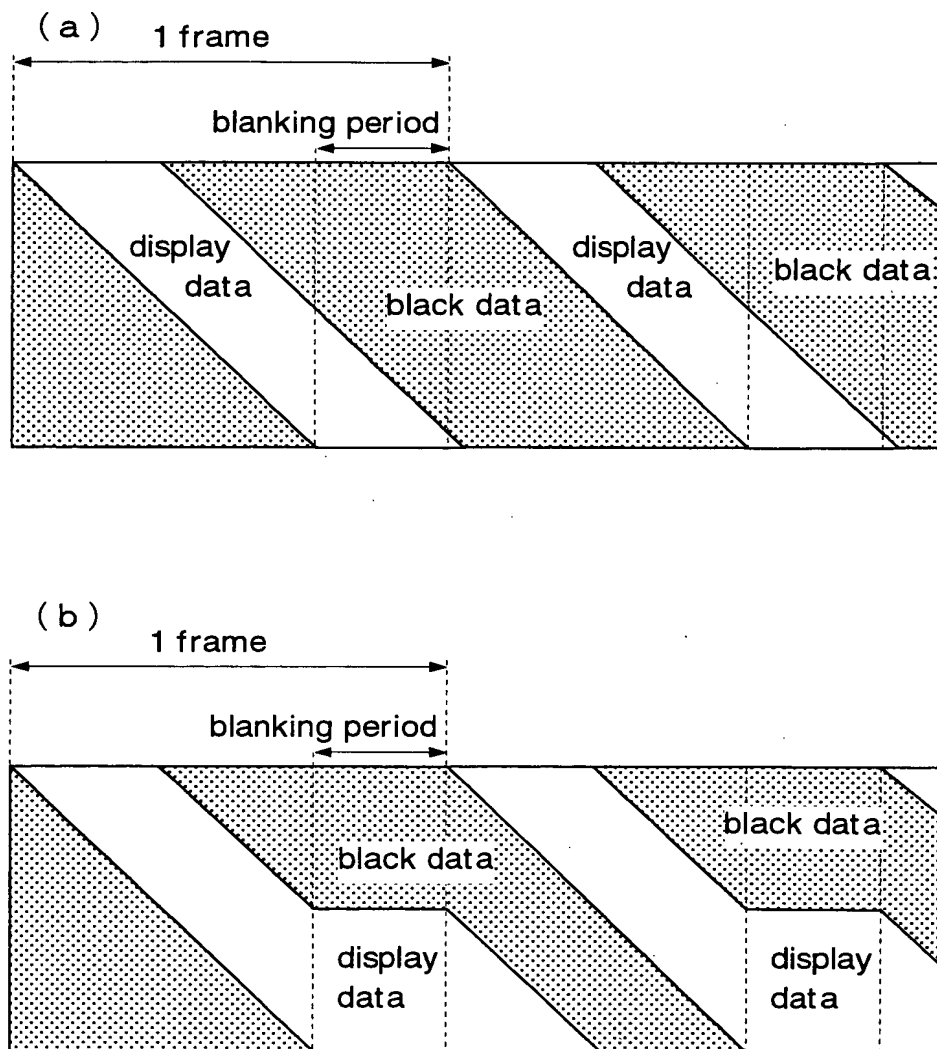


Fig. 70

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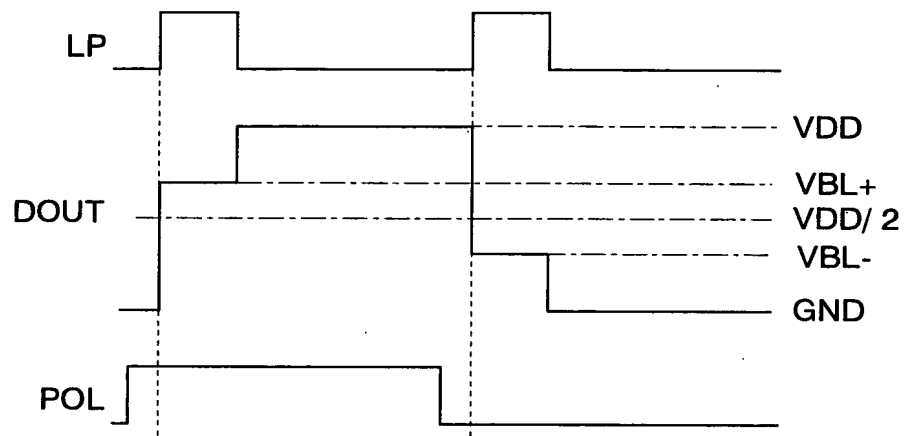


Fig. 71

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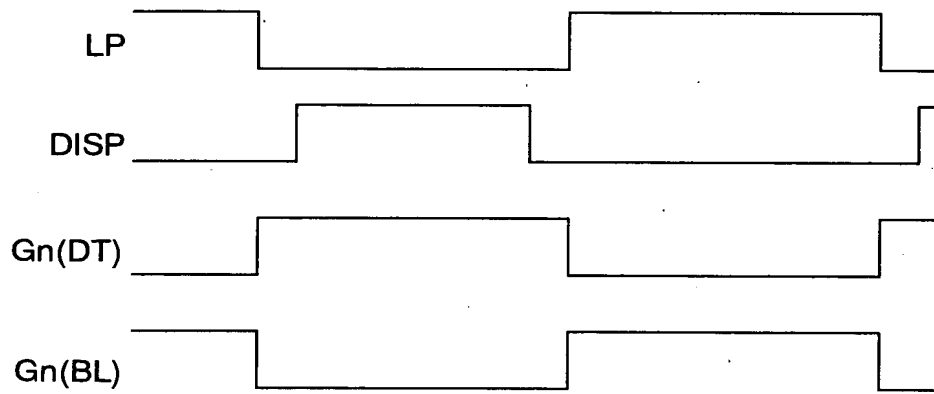


Fig. 72



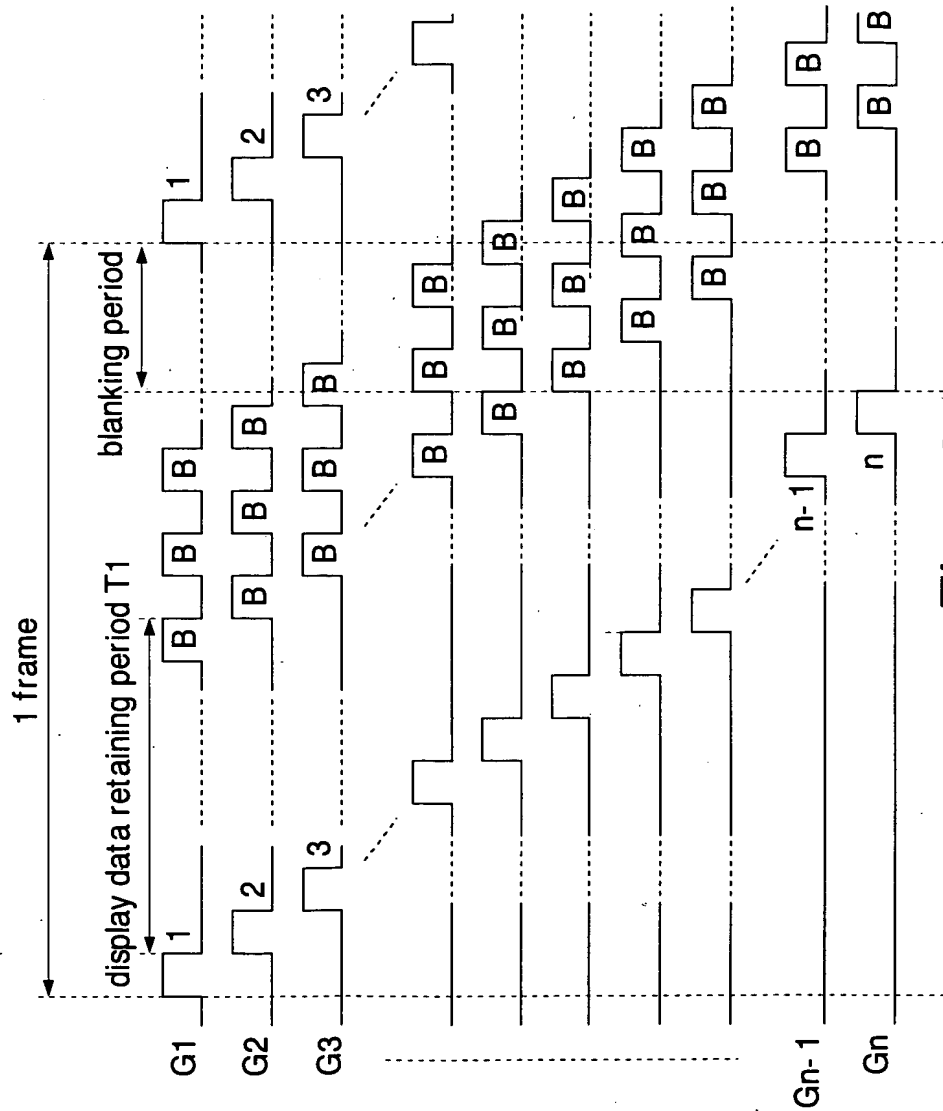


Fig. 73

display data

control circuit 142

X driver 16

D1 Dm

Y driver 14

G1 Gn

A C

141

141a

**Fig. 74**

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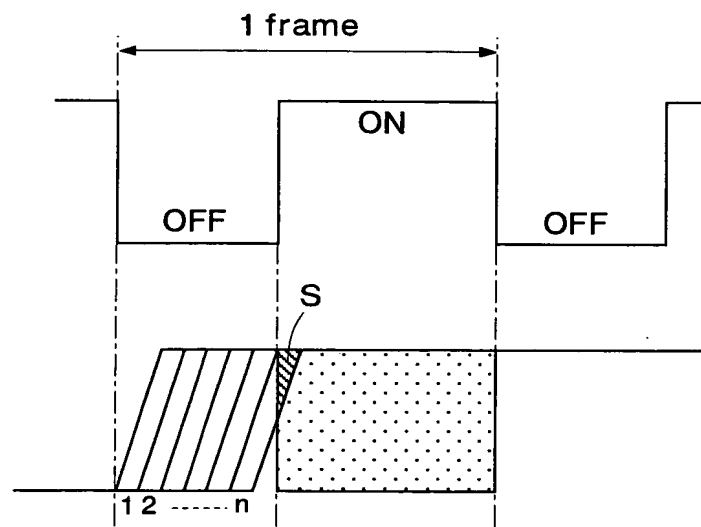


Fig. 75

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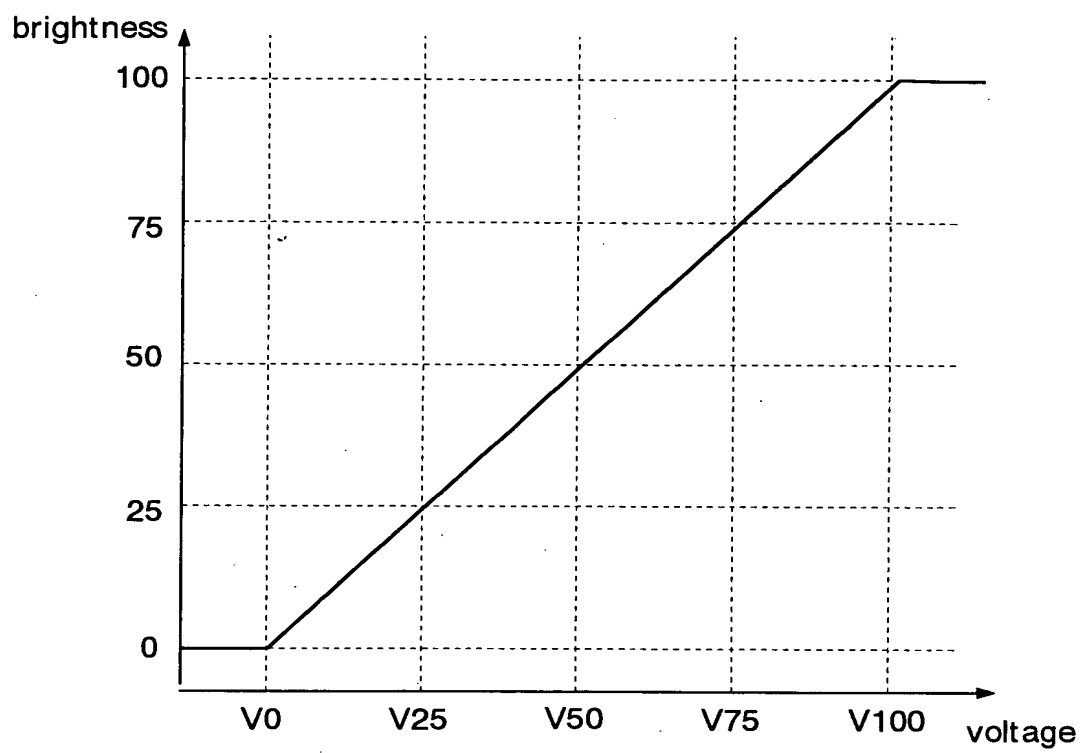


Fig. 76

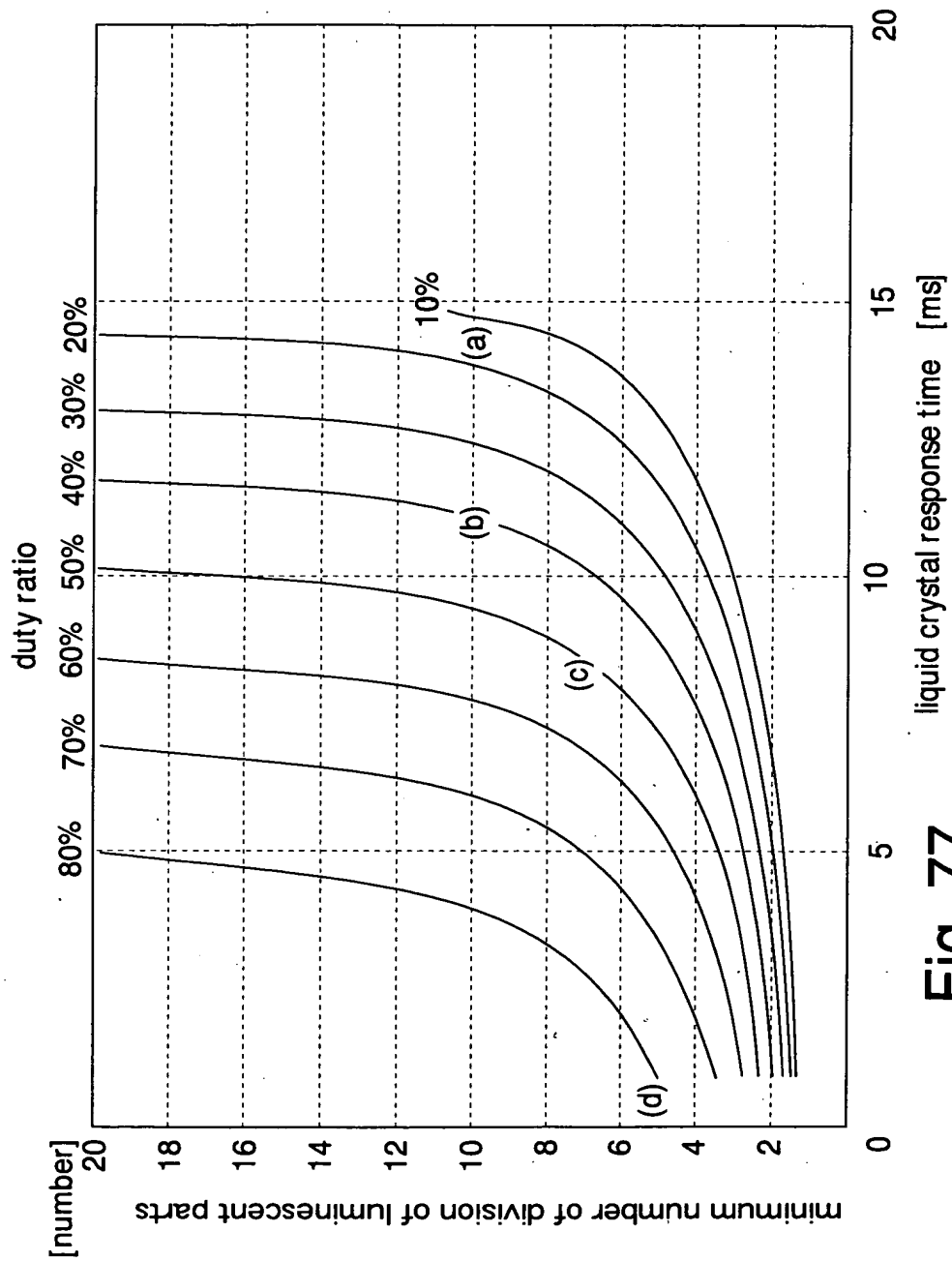


Fig. 77

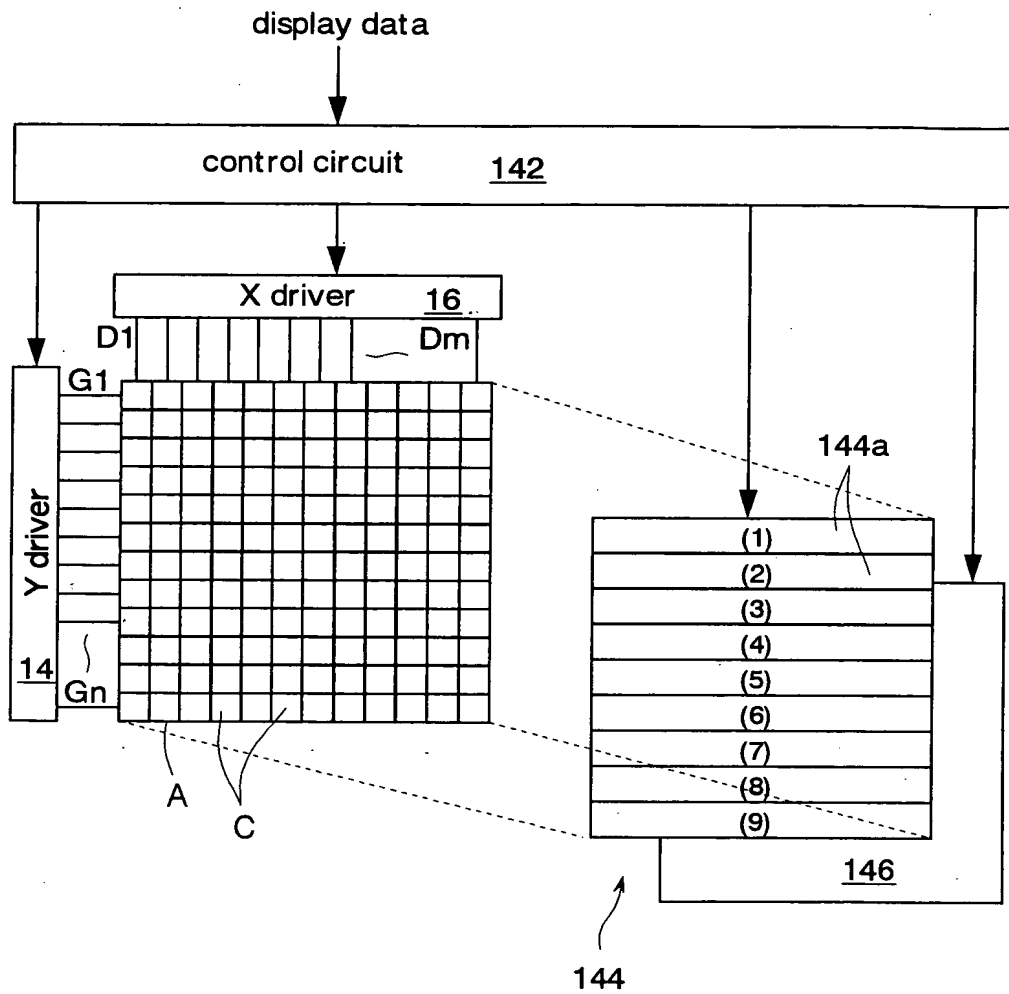


Fig. 78

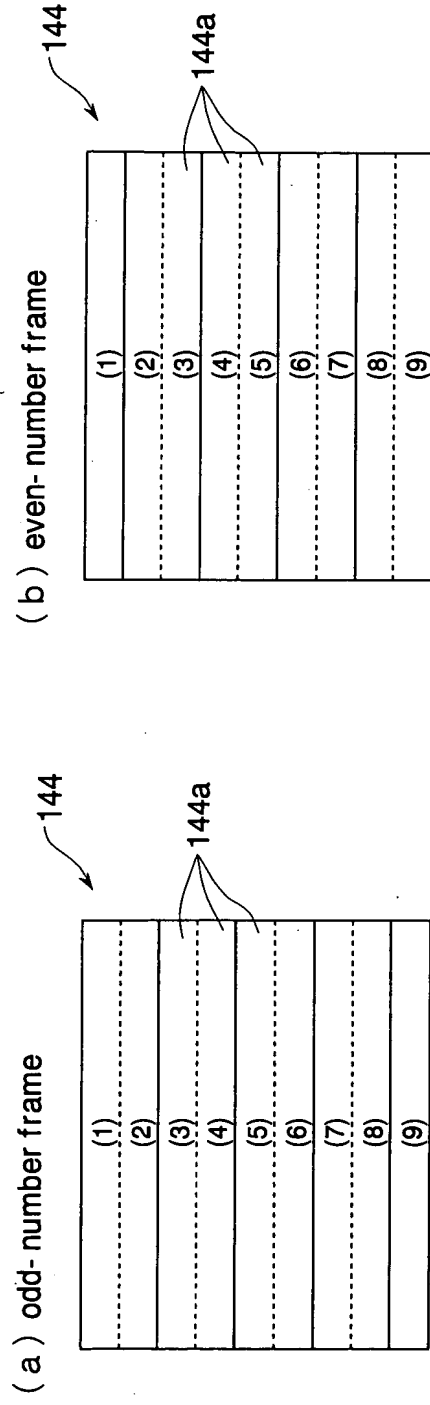


Fig. 79

display data

control circuit 148

150

X driver 16

D1 Dm

G1 Gn

Y driver 14

146

A C

**Fig. 80**



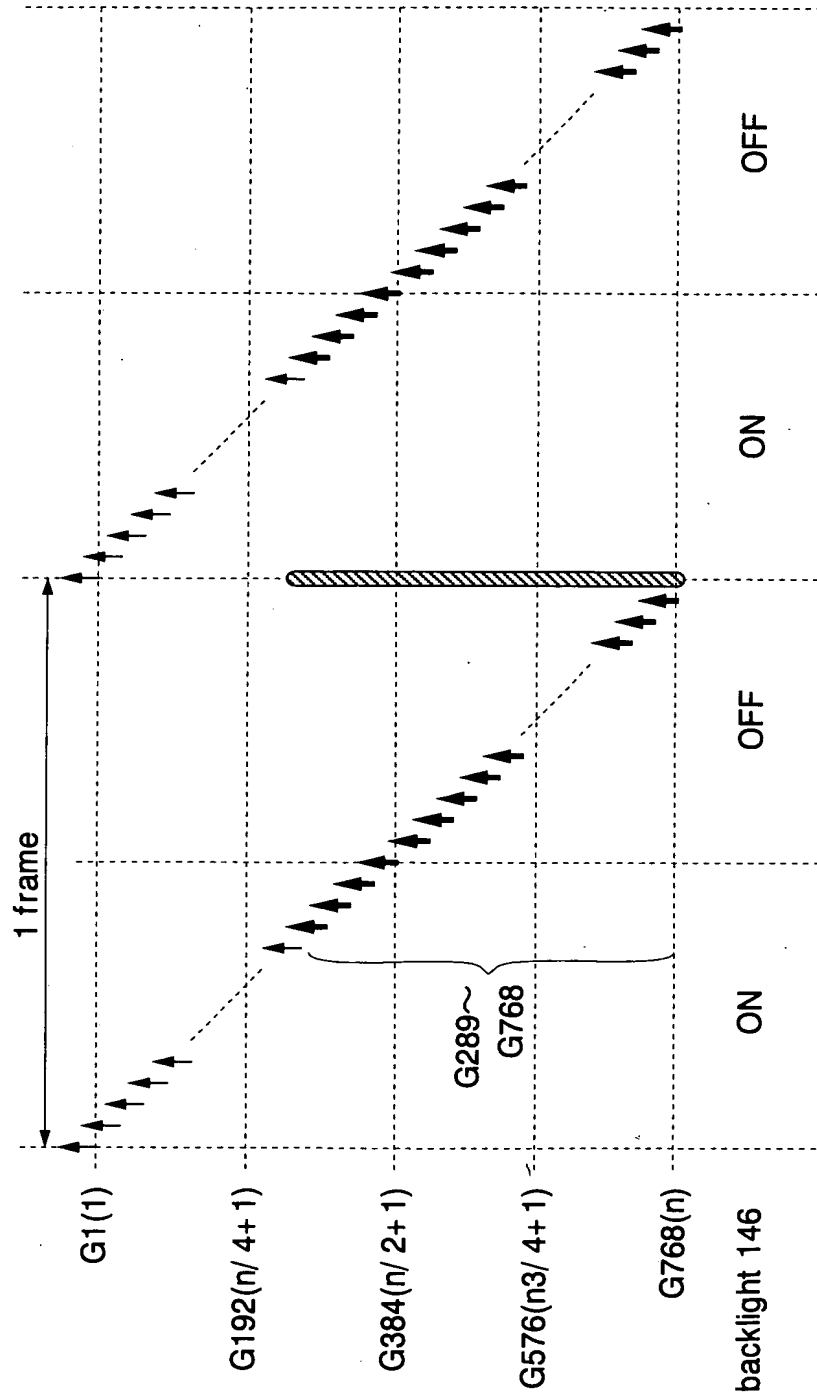


Fig. 81

**Fig. 82**